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Phase measurement technique for Synchronous devices in FPGA using XOR gates

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Abstract
Every Electronic system use PLL (Phase Locked Loop) that requires a clock signal and applications like clock and data recovery circuits for serial input output and RF transceivers, Analog to Digital Converter Spectrum analyzer, image processing, smart grid and radar. In our project we use Bang Bang phase detector i.e.) binary phase detector which has potential of use in high speed which can be implemented with a simple D flip flop and XOR gate. We also discussed the procedure of the phase measurement system, the calibration sequence involved, followed by the performance of the design in terms of timing issues i.e. skew and jitter using XOR gates to make this phase detector suitable for FPGA where there is a need to preserve the synchronous relationship between the clocks.

Keywords: PLL, phase detector, XOR, jitter

Introduction
Experiments use phase information to calibrate and synchronize signals between different circuit elements. In certain experiments such as in high energy physics (HEP), preservation of phase relationship between critical signals throughout the experiment runtime is a necessary condition. Nowadays the implementation of digital architecture and hardware techno like FPGA (Field Programmable Gate Arrays) play an important role. Gigabit transceiver and timing trigger are implemented in FPGA, which was used by HEP experiments. For the entire experiment we need latency critical protocol to maintain constant phase differences in the recovered signal. In each round of power cycle, loss of lock in the transceiver, reset cycle, aging of clock circuitry in PLL the high speed serial transceivers of FPGA don't maintain constant phase shift. Inside the FPGA circuitry phase shift of 20-100ps is needed in logic design for phase monitoring. This purpose is to extract the relative phase measurement and also for recalibrating the system when we needed, for the maintenance of the constant phase relationship. Literature discussed the several approaches for phase measurement Over sampling technique is an inadequate to measure a relative phase difference between the two high-frequency clocks inside an Field Programmable Gate Array (FPGA) fabric, whose frequency exceeding the maximum limit supported by the fabric (<500 MHZ). The solution for this work is to sample it externally using an analog-to-digital converter (ADC) and then feed it back to the FPGA or computation. This technique requires an additional hardware to measure the phase difference of the internal digital clocks. phase measurement approach had been achieved by using the Dynamic Phase Alignment (DPA) features of the FPGA PLLs. The drawback of this method is the achieved resolution, which is limited to the $1/8^{th}$ of the voltage-controlled oscillator (VCO) frequency. In this work, we propose a new method for an accurate phase measurement in a Field Programmable Gate Array (FPGA) by using subsamples that are collected by the systematic sampling over XOR-based phase detector (PD) single throughout this document and are identified in italic type, within parentheses, following the example. Some components, such as multi-leveled equations, graphics, and tables are not prescribed, although the various table text styles are provided. The formatter will need to create these components, incorporating the applicable criteria that follow.

Classical PLL
PLLs include carrier recovery, clock recovery, tracking filters, frequency, phase modulation, phase demodulation, frequency synthesis and clock synchronization which are an incomplete list of specific task.

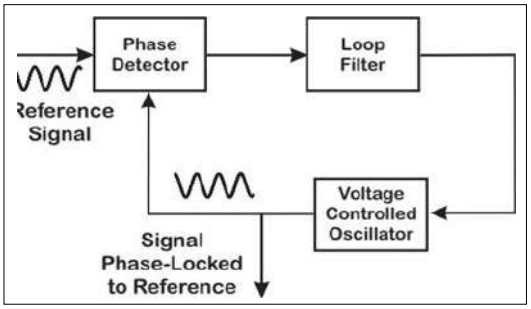


Fig 1: A general PLL block diagram

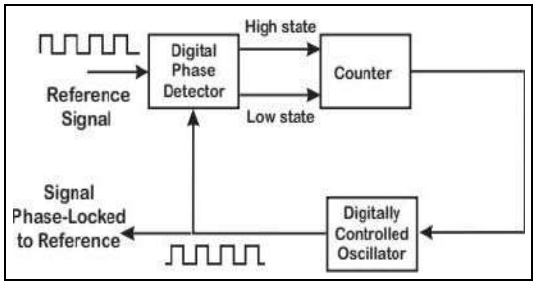


Fig 2: A classical digital phase locked loop

This diagram shoes the important component of every PLL must have, namely:

Phase detector (PD)
PD is a nonlinear device which produces an output that contains the phase difference between the two oscillating input signals.

Voltage controlled oscillator (VCO)
VCO is a nonlinear device that produces an oscillation whose frequency is controlled by a lower frequency input voltage.

Loop filters (LF)
Phase locked loops (PLLs) are applicable in radio, television, communications (Wireless, telecom, datacom), storage devices, noise cancellers and the like for that wide spread using of such storage devices, PLLs are the most ubiquitous form feedback system built by engineers Proper functioning of PLL depends on low pass filtering.

A feedback connection
Normally the binary phase detector uses its input as the reference signal and the output of the Voltage controlled Oscillator (VCO). The phase error (PE) i.e. output from phase detector, used as the control voltage for VCO. The PE may or may not be filtered. In control system perspective the PLL have several unique characteristics. Correct operation of all the devices in PLL depends on their nonlinearity. Without PD and VCO there is no loop. Both of these elements translate the response from signal to phase and back again. By taking this is as a time scale shift, as PLLs typically operate on signals whose Centre frequency is much higher than the loop bandwidth. Secondly, PLLs are almost always low order. Without taking various high frequency filters and parasitic poles, most of the PLLs in the literature review are first or second order. In few applications where third or fourth orderly oops are used, but it form risky and sophisticated devices. So all the components in PLL was designed and specified by designer except motor that was controlled by PL. Thus, complete feedback loop is governed by required characteristics of the input reference signal, the required o/p signal and limitations of the circuit's technology. The control of motors using PLL depends on the designer's Prudence.

Digital PLL
A classical digital phase locked loop. There is a straight forward definition for the most digital feedback loop. Digital loops use ADC to convert samples into digital quantity and computer to perform calculation and DAC to output the control signal. Operation of a digital PLL depends upon which text to be reader. Except phase detector all the components in digital PLL was analog. In other cases, the loop consists of a digital phase detector, a digital filter, and a numerically controlled oscillator. Software creation of PLL is possible if the entire input signal is digitized. In DPD (Digital Phase Detector), both all-digital PLL and classical digital PLL are used. The DPD's output may be either pulses or multi bit values in ADPLL. The ADPLL replaces the analog filter to digital filter and VCO (Voltage control oscillator) into a DCO (Digital control oscillator).

Software PLLs
In software PLL's, the implementation in software can be done faster than the loop centre frequency. It has the advantage of flexibility. Any type of PLL provides the sample rate in high enough. Software loops deal with real data. Software PLL's may operate in on both data in real time and post processing of measured data. One of the cautionary effect to be noted in hardware such as limiters having high frequency which creates real sampling issues for software loops.

Phase detectors
One of the properties of phase detector is that when an ideal multiplication is done ones, the base band signal can be analyzed more rigorous. The phase detectors are constructed from digital logic for the initial reduction of phase band relies in pulses width modulation and averaging. Even though they have better pull in range and are more manufacturable for high speed applications but they have worse noise performance than the classic mixing detectors. In most of these phases detectors have their low frequency in linear range than sinusoidal. From the analysis the Digital phase detectors require a different view from the classical mixing detectors. Finally phase detector is not best suited for all situations. So the different circuit designs are chosen largely to do the same functionality in various applications.

Classical mixing phase detector

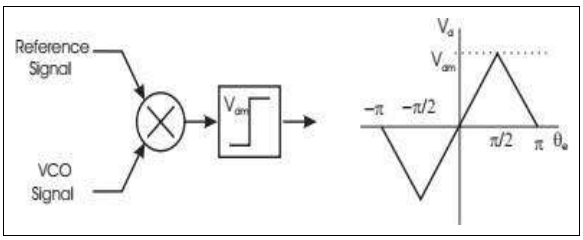


Fig 3: Classical mixing phase detector

PLL applications include Balanced Mixers which are used in the microwave frequency range as well as in low noise frequency synthesizers. This results in a loop whose gain is dependent upon the amplitude of the signal. Also, an non idealities in the circuit implementation of the mixer result in responses those are far from linear. An issue, it has an advantageous to move to a detector which has an immunity

for those effects.

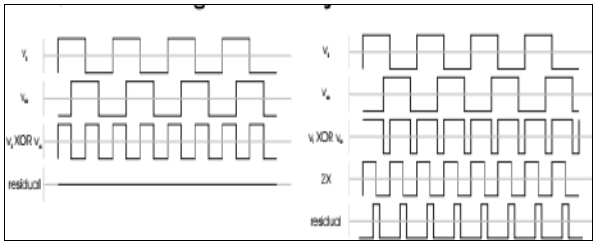


Fig 4: Phase detection using an XOR gate. Note that this accomplishes the same things as an overdriven mixer, but with digital circuitry

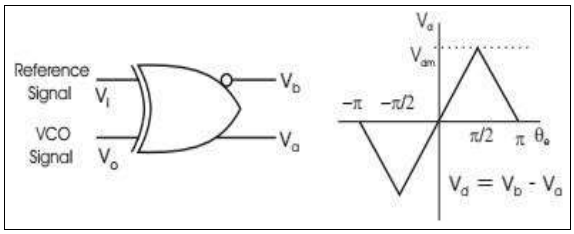


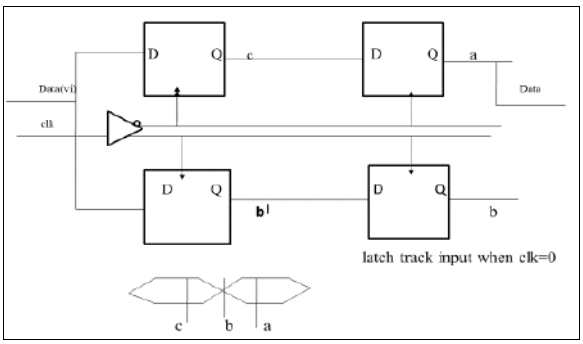
Fig 5: Phase detection using a XOR gate. On the left, a phase shift between reference and VCO output of π/2 produces an output of the phase detector whose baseband component is 0. On the right a baseband components 0. On the right a relative phase shift of π/4 results in an output of the phase detector whose baseband component is vd/2. The output is broken up here into a 2X frequency signal and a residual. The 2X signal averages to 0, while the residual averages to the baseband phase error.

For a variety of reasons, it may be desirable to have loop which does not produce a sinusoidal clock but instead a square wave clock. If the mixer circuit is over-drived by one, hat is if the signals are used by one so large that the amplifiers saturate, the output signals stop looking like sinusoids and start looking like Walsh functions (rectangular signals). Such a phase detector is shown in Figure 10.Understanding the output of a Phase Detector (PD) relies on a combination of averaging analysis and heuristics. However, one of the more interesting features of such a phase detector is that it can be implemented using an Exclusive-OR (XOR) gate as shown in Figure 11. In this method, one advantage of such a Phase Detector (PD) is that the loop gain is now independent of input signal amplitude.

Two state phase detector

The mixing (i.e. multiplying) phase detector operates on the entire range of input signal and VCO signal due to that it has superior noise performance than any other detector discussed here. Balanced mixer is the best option for PLL application especially when it operates in microwave frequency & synthesizer in low frequency. But the resulting circuit far away from non-linearities and its loop gain depend on the signal amplitude. So there is necessity for making a detector which has more immunity to the above mentioned effects.Secondly, the linear region of the phase detector is expanded to ±π from ±π/2.Finally, the phase detector is no longer memory less. Thus, noise spikes that are large enough to trigger a change of state have a larger effect than they do with the XOR phase detector. Because this phase detector uses only the leading edge of the input signals, the linear region is increased as mentioned above. The resulting baseband response can be understood from square wave manipulations an described above sawtooth detector.

Bang-bang clock phase detector

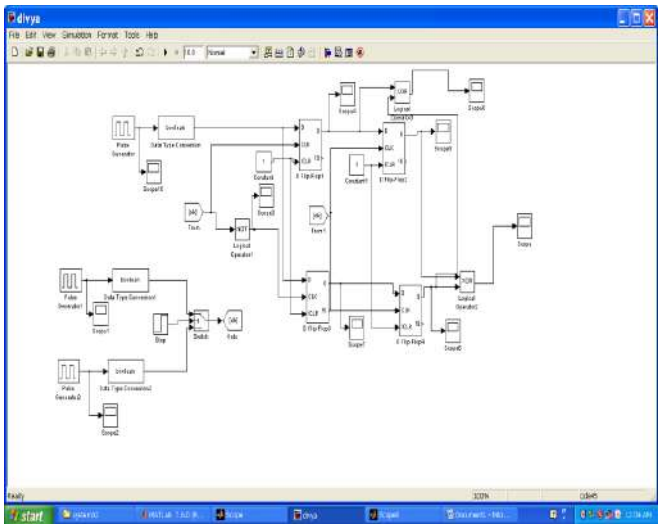


c = a; There is no phase shift, c ≠ a; Output is based on b, b = a; The clock is early, b = c; The clock is late.

Fig 6: The Alexander (bang-bang) phase detector. The original version made of component flip flops. The version shown here is a circuit well suited to integration which substitutes a latch for the last flip flop, thereby saving one latch. On the right is the phase detector characteristic.

This the implementations view of Bang-Bang phase detector. It has a capability of High pull in range as well as able to detect the reason for phase shift such the late or early arrival of clock 4. This section shows the how the XOR gate 6 is suitable for phase shift. Pulse generator Figure 7: Output window of pulse generator [clock] to D-flipflop XOR gate Figure 9: Output window of XOR gate it shows one which means there is 1 phase shift between the input and output. Calculation: In this section we are calculating the phase angle for various duty cycle.

Implementation



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This the implementations view of Bang-Bang phase detector. It has a capability of High pull in range as well as able to detect the reason for phase shift such the late or early arrival of clock.

1. This section shows the how the XOR gate is suitable for phase shift.

Pulse generator

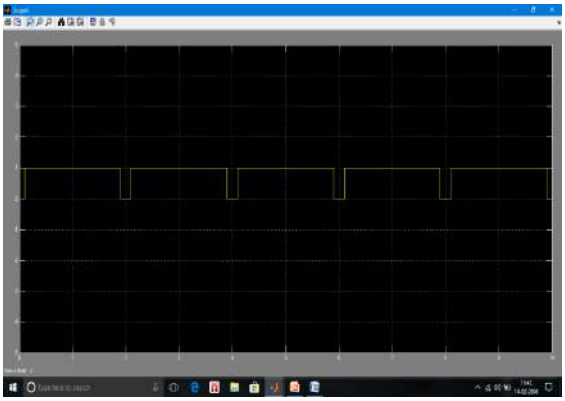

Fig 7: Output window of pulse generator

[clock] to D-flipflop

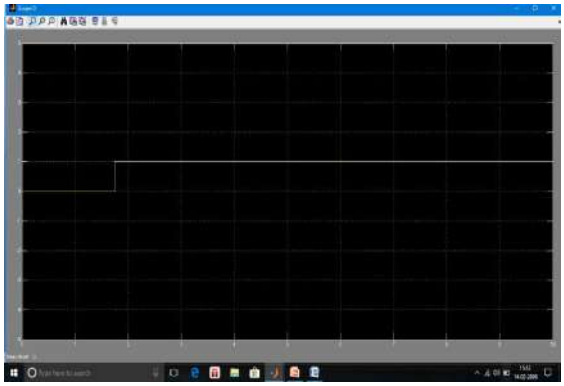

Fig 8: Output window of clk to the D flip flop

XOR gate

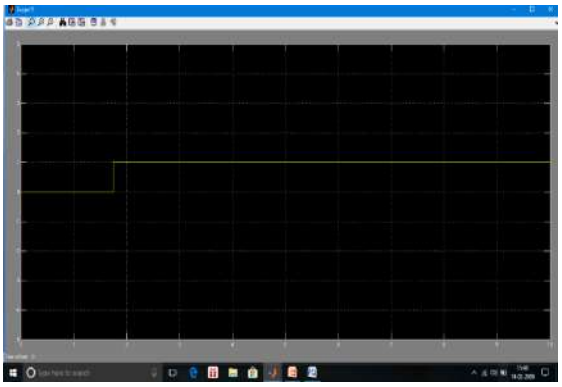

Fig 9: Output window of XOR gate it shows one which means there is phase shift between the input and output.

Calculation

$x(t) = \sum_{n=-\infty}^{\infty}$ ((u[t - nT + DT2] - u[t - nT - DT/2]) (1)

So clk1, T = T/ 2, t + tθ = t, Dθ1 = D (2)

$x(t) = \sum_{n=-\infty}^{\infty} =$ (u[t - nT/2 + Dθ1T/4] - u[t - nT/2 - Dθ1T/4]) (3)

Where duty cycled = 12 or 50% and time period T = 1 f0 Similarly, the digital clock (CLK2) having the same frequency (f0) and shifted by the t0 phase is given by x[t + tθ].
So clk2, T = T/2, t + tθ = t, Dθ2 = D

x (t + tθ) = Σn = -∞ (u[t - nT/2 + Dθ2T/4] - u[t - nT/2 - Dθ2T/4]) (3)

The phase difference between CLK1 and CLK2 is calculated by the XOR - based PD. There resulting XOR waveform y (t) Equation (2) & (3) combined by,

x (t) = y (t) ⊕ x (t + tθ)
y (t) = Σ∞n = -∞ (u[tnT2 + Dθ1T4] - [tnT2 - Dθ2T4]) (4)

Where Dθ1 = 0, Dθ2 = tθT2, tθ < T2
Dθ1 = θT2, Dθ2 = 0, tθ ≥ T/2 (5)

This a pulse drain of duty cycle Dθ, composed of two independent variables Dθ1 and Dθ2.The full duty cycle Dθ is given by (5), as the ratio of the phase difference (t) to the half-time period T2. Continuous-time signals y(t) and x(t) are uniformly sampled by the sampling clock of time period T to obtain the discrete time signals y[kTs] and x[kTs] respectively. The number of samples acquired for phase computation is referred as the sample population size (N). The ratio (R) of the mean of N number of samples for the discredited XORed signal to the reference clock (CLK1) is given as

R = NΣK = 1y[kTs]/NΣK = 1x[kTs]

This ratio (R) tends to a constant value as the sample population size (N) increases, as seen in the following equation:

RN→∞ = DθD = Dθ1 + Dθ2D

The phase difference tθ can be calculated from reaeration, replacing = 1/2 from (1) and Dθ = (tθ/T/2) from (2). The relationship between tθ and R is shown below where R can take any value within the range of [0-2]

RN→∞ = Dθ/D = Dθ1 + Dθ2/D
Dθ1 + Dθ2 = D
= tθ/T/2/D
= tθ/T/21/2
= tθ/4/T
= T/4 × R

The phase shift measurement represented in Angular from replacing T/4 with 90°

θ˜ = 360° × tθ/4 × R

tθ = T/4 × R to value is substituted by,

θ˜ = 360° × T/4/4T × R

The phase shift measurement represented in angular from replacing T/4 with 90°

θ˜ = 360° × tθ4 × T
tθ = T/4 × R to value is substituted by,
θ˜ = 360° × T/4/4/T × R
= 360° × 1/4 × R
= 90° × R
tθ = T 8 × R
θ˜ = 360° × T/8/4/T × R

Output

Variation in the clock edge (either clock early are late) is used to identify the phase shift. This is the output from Bang-Bang phase detector it shows whether the give clock is early or late.

c-output

Fig 10: This is the C output of Bang Bang phase detector

a-output

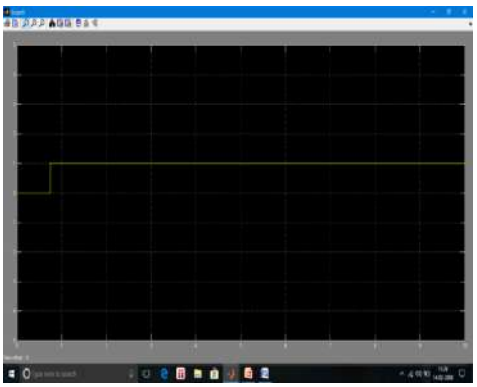

Fig 11: This is the A output of Bang-Bang phase detector. Both c and a clk edge position are same i.e. there is no phase shift.

b-output

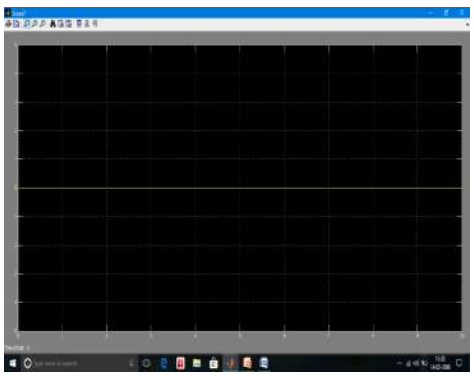

Fig 12: This is the b output to Bang-Bang phase detector. Output b = a only when there is a phase shift due clock early. Here its how zero output because there is no phase shift

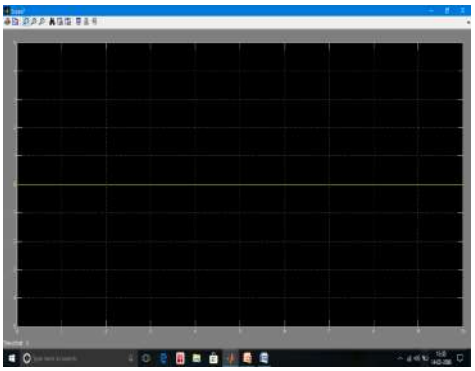

Fig 13: This is the b output of Bang-Bang phase detector. Output b = c only when there is a phase shift due clock late. Here its how zero output because there is no phase shift.

Experiment: 2

Here we are conducted an experiment to detect the Out of phase waveform.

C

Fig 14: This is the C output of Bang Bang phase detector

a

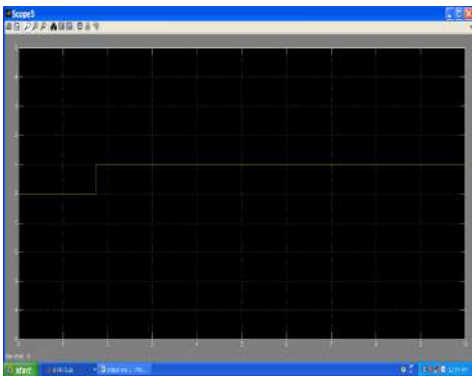

Fig 15: This is the A output of Bang-Bang phase detector. Both c and a clk edge position are not same i.e. there is phase shift

Fig 16: This is the b output of Bang-Bang phase detector. Output b = c only when there is a phase shift due clock late

Application of phase detector

Disk drive control

In sectored servo - the dominant format for modern hard disks - the clock must be recovered at the beginning of each sector. Although the most common encoding is called amplitude encoding, an alternate example uses phase encoding of position error. In this case the phase difference between the reference mark and the position mark gives a measure of the cross track position.

Motor control

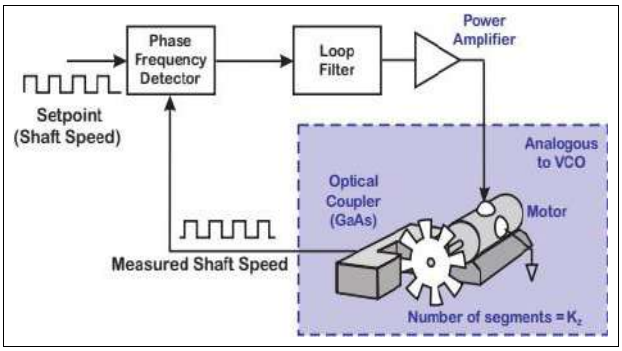

Fig 17:

There are several interesting points about PLL based motor speed control. First, the motor model itself is second order (rather than the first order model of the VCO).

Conclusion

In this paper, we have discussed the development of a sensitive phase detection logic core for FPGA, having precision, accuracy, and resolution in the range of a few picoseconds. This can be used within FPGA as a monitoring device of phase relationship between digital clock pulses, without any additional circuitry. The design is modularized in a way that allows designers to modify different components for more robustness of the design, like replace XOR- based PD with other phase comparator. The concept of using systematic sampling for subsample collection can also be extended to map other complex analog domain problem to digital domain.

References

1. Gupta SC. "Phase-locked loops, "Proceedings of the IEEE 1975;63:291-306.
2. Lindsey WC, Chie CM. "A survey of Digital Phase-locked loops, "Proceedings of the IEEE 1981;69:410-431.
3. Gardner FM. Phase lock Techniques. New York, NY: John Wiley & Sons, second ed 1979. ISBN 0-471-04294-3.
4. Blanchard A. Phase-Locked Loops. New York, NY: John Wiley & Sons 1976.
5. Viterbi AJ. Principles of Coherent Communication. McGraw-Hill Series in Systems Science, New York, NY: McGraw-Hill 1966.
6. Wolver DH. Phase-Locked Loop Circuit Design. Advanced Reference Series & Biophysics and Bio engineering Series, Englewood Cliffs, New Jersey 07632: Prentice Hall 1991.
7. Brennan PV. Phase-Locked Loops: Principles and Practice. New York: McGrawHill 1996.
8. Best RE. Phase-Locked Loops: Design, Simulation, and Applications. New York: McGraw-Hill, thirded 1997.
9. Crawford JA. Frequency Synthesizer Design Handbook. Norwood, MA 02062: Artech House 1994.
10. Bodson M, Jensen JS, Douglas SC. "Active noise control for periodic disturbances," IEEE Transactions on Control Systems Technology 2001;9:200-205.
11. Adkinsand CA, Marra MA. "Modeling of a phase-locked loop servo controller Within coder feedback, "in Proceedings of IEEE Southeastcon'99 1999, 59-63. IEEE.
12. Lindesy WC, Simon MK eds. Phase-Locked Loops and Their Application. IEEE PRESS Selected Reprint Series, New York, NY: IEEE Press 1978.
13. Lindesy WC, Chie CM eds. Phase-Locked Loops. IEEE PRESS Selected Reprint Series, New York, NY: IEEE Press 1986.
14. Razavi B ed. Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design. IEEE PRESS Selected Reprint Series, New York, NY: IEEE 1999.