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Design of an efficient adders for signal processing applications

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Abstract
An adder is a digital circuit that simply performs addition of numbers. In many Personal computers and different kinds of processors, adders are deployed in the arithmetic and logical units or ALU. They are additionally utilized in different pieces of the processor, where they are employed to compute addresses, indices of tables, incrementation and decrementing process in operators and similar operations in the hardware. Error Tolerant Adder (ETA) is a kind of adder which sacrifice its accuracy to improve its speed and area. The power delay product is the average product of power consumed and worst-case delay is improved. By lessening the power consumed, the battery life of any portable device can be improved. This project presents the design of high speed and area efficient adders which include Ripple carry adder (RCA), Carry look ahead adder (CLA), Carry skip adder (CSA), Kogge stone adder, Brent Kung adder each incorporated with the Error tolerant adder (ETA) and compared the speed, area power utilized by each adder with and without incorporating ETA. The results are tabulated to show the variation in speed, area and power for different adders.

Keywords: Error tolerant adder (ETA), low-power and high-speed circuit, VLSI

Introduction
Essentially, in VLSI chip configuration signal handling is executed for viable coordination in the framework. In present age, integration assumes significant part to get compelling yield. In VLSI design, essentially energy and area assume significant part in the whole framework. These two parameters are required to decrease the energy utilization. The frequency of operation and capacity of chip is worked in the framework with the end goal of development. By utilizing cooling methods, the energy utilization is resolved. In electronic gadgets the battery life assumes significant part in the framework. There shall be an impediment for battery life and the activity time is additionally delayed in the whole framework. In the applications of signal processing, operation of multiplication assumes significant part in whole framework. By utilizing adders, energy and latency is impressive. In VLSI, adders give low energy utilization. Logic levels and circuit in multipliers is broadened and area is exploited. To perform fast tasks, multipliers are placed in parallel manner. Adders are characterized dependent on two multipliers. They are completely parallel adders and completely serial adders. Here by utilizing this, both area and speed is worked at profoundly. In advanced PCs and computerized signal processor, the addition operation is performed successfully. Arithmetic operations are done in the essential structure blocks which assumes significant part in whole framework. In equipment engineering, ALU unit assumes significant part. Various characteristics and various architectures are existed to implement the arithmetic tasks.

Existed system
Ripple-Carry Adder (RCA): The n-bit adder is worked from n-one bit full adders is known as ripple carry adder, in view of how the carry is processed. Each 3 bit adder inputs a C carry, where is the Cout carry out of the past adder. This sort of adder is a RCA, because each carry bit "ripples" to the following full adder.

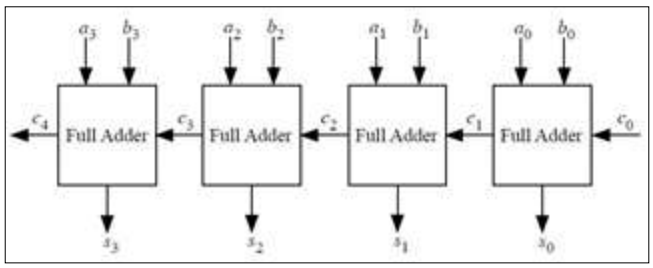

Fig 1: 4- bit RCA

This adder is basic, which considers quick design time, but this adder is moderately slower, given that each full adder should hold on for the carry to be determined from the past full adder. This adder requires three degrees of logic. In a 32-bit (ripple carry) adder, there are 32 full adders, so the basic way, delay in the worst case is 31 * 2(for propagation of carry) +3(for sum) = 65 gate delays.

Carry look-ahead adder CLA: CLA logic utilizes the ideas of generation and propagation of carry. The addition of two 1-bit inputs A and B is said to create if the addition will consistently carry, whether or not there is an input carry. On account of twofold (binary) addition, A+B propagates if and just if both A and B are 1. The addition of two individual bit inputs A and B is said to propagate if the addition will carry at whatever point there is an input carry. The propagate and generate signals are characterized regarding a solitary digit of addition and don't rely upon some other digits in the entirety. On account of twofold addition, A+B propagates if and just if in any event one of A or B is 1. By this definition, A+B is said to propagate if there is an input carry, yet won't carry if there is no input carry. For binary arithmetic operations, or is quicker than xor and takes less transistors to execute. However, for a multiple level CLA, it is simpler to utilize.

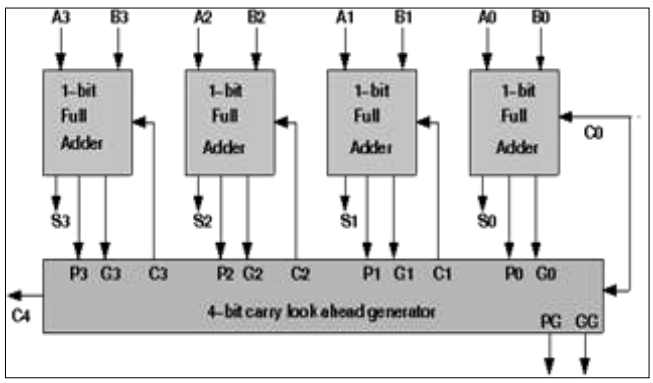

Fig 2: CLA This adder addresses the most broadly utilized for fast adders in present day PCs. The upside of utilizing a look-ahead design over a RCA is that the Look-ahead is quicker in processing the solution

Carry skip adder (CSA): The CSA comes from the gathering of a by-pass adder and it utilizes a RCA for a adder execution. The development of CSA block is acknowledged by improving delay in the worst case. This adder is a capable one as far as to its usage of area and power utilization. This adder might be executed either utilizing FSS or VSS procedure where the maximal speed might be accomplished for the VSS structure. The size of the stage is equivalent to the RCA block size. In FSS procedure, the size of all of the stages are same. In VSS procedure, the size of all stage contrasts from each other. By allocating variable sizes to the stages, the speed of the adder construction can be improved. The speed improvement can be acknowledged by bringing down the delays of the first and third blocks. These delays are diminished by lessening sizes of first and last RCA blocks.

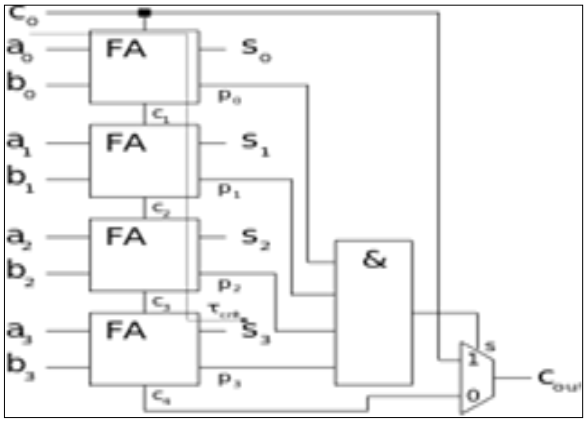

Fig 3: 4-bit CSA

The Kogge-Stone adder: It is a parallel prefix form of CLA. It generates the carry signals in O(log2 N) time, and is widely concluded as the fastest adder design available. It is the most common architecture for high-performance adders in industry. This adder's concept was first developed by Peter M. Kogge and Harold S. Stone (Javed Ashraf and Madhu Thakur in 2012). In Kogge-stone adder, carry is generated quickly by executing them in parallel at the cost of maximization of area. The Kogge-Stone adder can be modified by lessening the Black cells and rerouting to fulfill the functionality of adder.

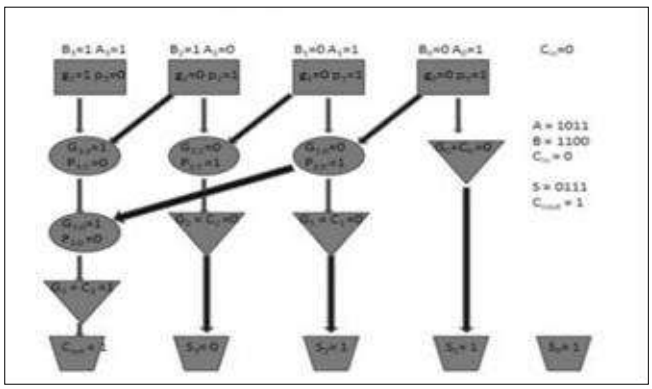

Fig 4: Kogge stone adder

Brent-Kung adder: is a parallel adder made in a common layout with a goal of reducing the chip area and ease of production. The addition of n-bit number can be done in time with a chip size of area thus making it a good-choice adder with limitations on area and increasing the performance. Its similar and common build structure minimise costs effectively and enable it to be used in pipeline architectures. In parallel adders the critical path is decided by computation of the carry from least significant bit (LSB) adder to the most significant bit (MSB) adder, therefore number of computations are being reduced the critical path for the carry to reach the MSB

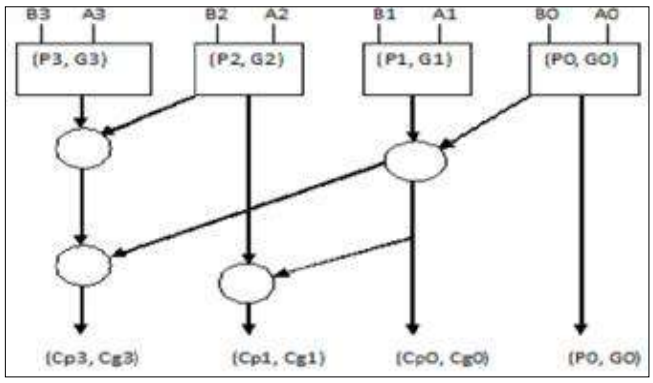

Fig 5: 4-Bit Brent Kung Adder

Proposed System

The outline of the equipment execution of such an Error Tolerant Adder that receives our proposed addition tasks of arithmetic operations is given. This most clear design comprises of two sections: a precise part and an erroneous part. Fig 6 represents the block diagram of ETA. The exact part is developed utilizing an ordinary adder like the RCA [7]. The carry in pin of this adder is associated with ground. The erroneous part comprises two parts: a carry free addition block and a control block. The Control block is utilized to produce the control signals, to decide the functioning method of the carry free addition block [1]. A 64-bit adder is utilized as an illustration for outline of the design methodology and circuit execution of an Error tolerant adder.

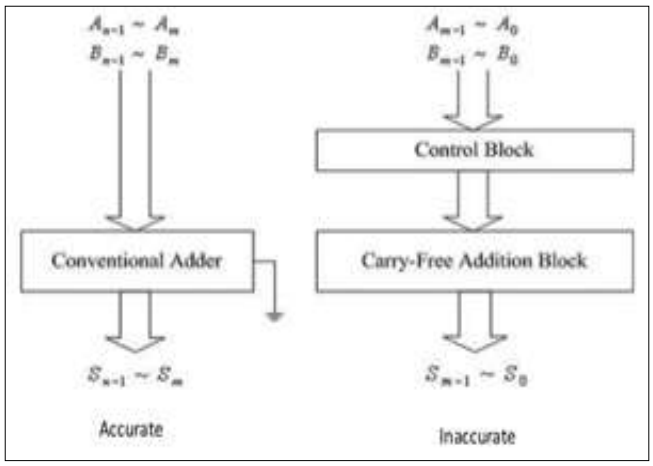

Fig 6: Block diagram of Error tolerant adder

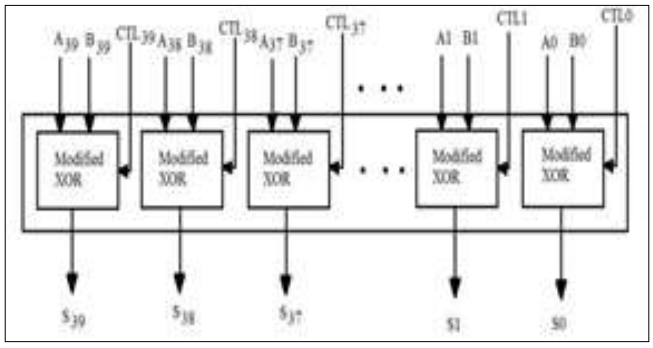

Fig 7: Block diagram of carry free adder of ETA

The erroneous part is the most basic part in the proposed ETA as it decides the precision, speed execution, and utilization of power of the adder [3]. The erroneous part comprises of two parts: the carry free addition block and the control block. The carry free addition block is comprised of 40 modified XOR gateways, and every one of which is utilized to generate the whole sum [8]. Fig. 7 shows the Block diagram of carry free adder of ETA

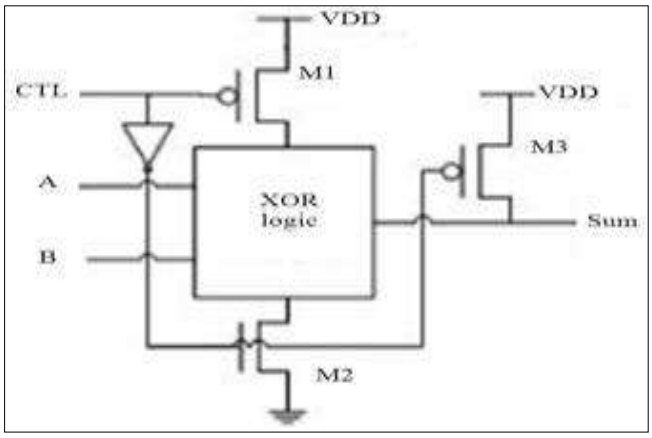

Fig 8: Modified XOR gate

In the modified XOR gateway, three additional transistors, M1, M2, and M3, are added to conventional XOR gate. Fig 8 shows the schematic of Modified XOR. CTL is the control signal coming from the control block and is utilized to set the operational method of the circuit [5]. At the point when CTL=0, M1 and M2 are turned on, while M3 is terminated, leaving the circuit to work in the ordinary XOR mode.

Control block

The aim of the control block is to identify the first bit position when both input bits are "1," and to set the control signal on this situation just as those on its right side to high [10]. Fig 9 shows the Control block Structure of ETA. It is comprised of 40 control signal generating cells (CSGCs) and every cell produces a control signal for the modified XOR gate at the comparing bit position in the carry free addition block [4].

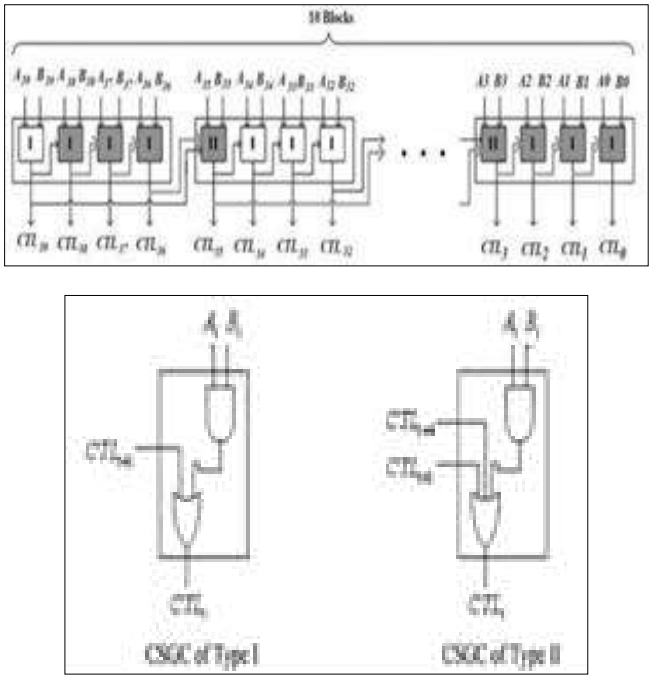

Fig 9: Control block structure

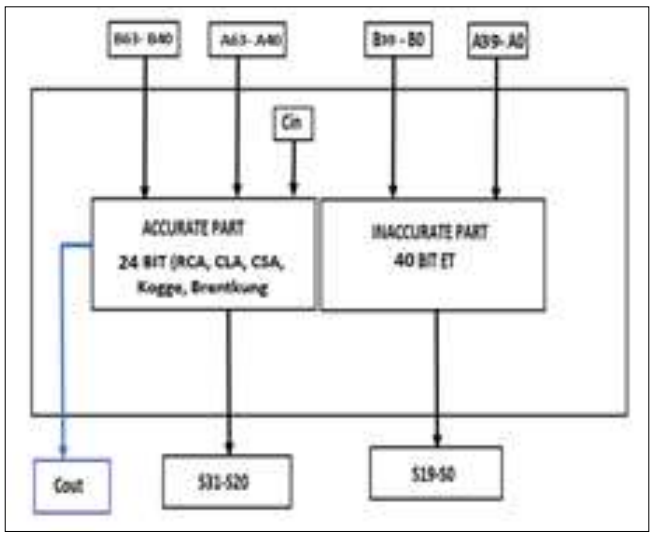

Fig 10: Block diagram of Error Tolerant adder with different adders

4. Results and Discussion

All the synthesis and simulation results are performed utilizing Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.7. The simulation results of RCA, CSA, KSA and BKA are appeared in underneath figures.

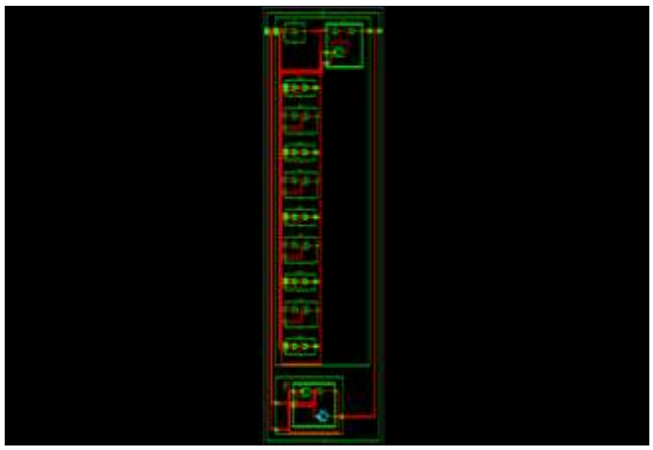

Fig 11: RCA with ETA (RTL schematic)

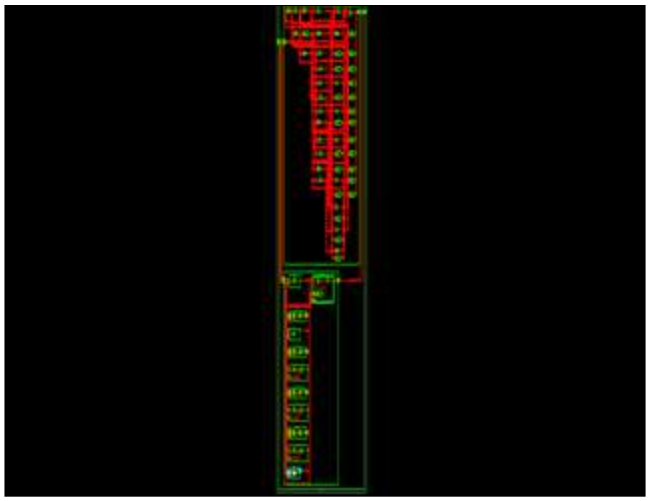

Fig 12: CSA with ETA (RTL schematic)

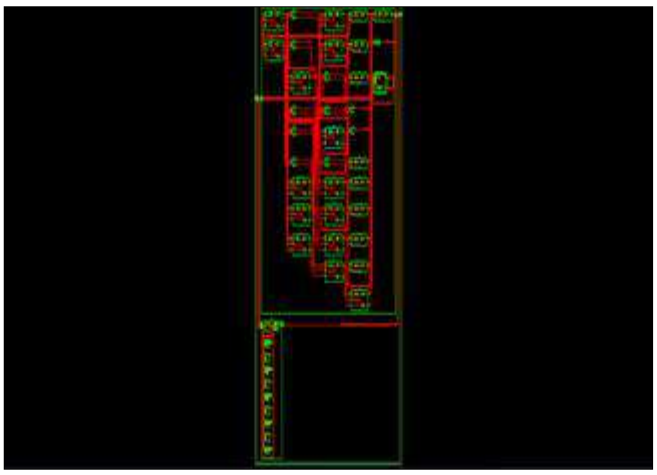

Fig 13: Brent Kung adder with ETA (RTL schematic)

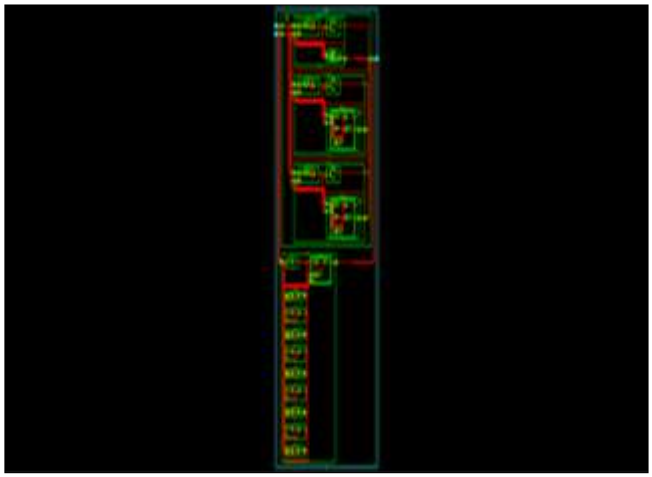

Fig 14: Kogge stone adder with ETA (RTL schematic)

Delay Comparison

The Fig 15 demonstrates the Delay variation of the different adders with and without ETA.

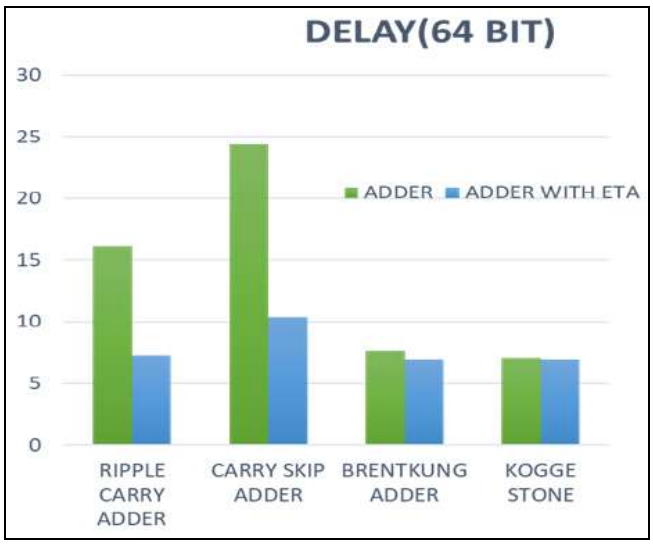

Fig 15: Delay comparison of adders

Area comparison

The Fig. 16 demonstrates the XOR gate comparison of the different adders with and without ETA.

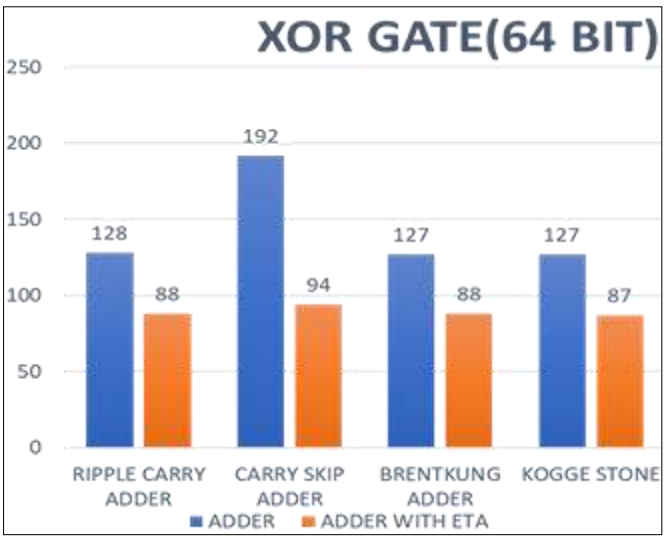

Fig 16: Delay comparison of adders

5. Conclusion

In VLSI circuit design there are few parameters that are very much important in determining the efficiency or the ability of the device, such as area, usage of power, delay and reliability. Different adders had advantages of their own. This project presented the combination of various adders implemented with Error tolerant adder and compares the various results, such as number of XOR gates of adders and delay with and without ETA.

The proposed Error Tolerant Adder trades a certain amount of accuracy for significant area saving and performance improvement.

The useful applications of the ETA fall mainly in areas where there is no strict requirement on accuracy or where super low power consumption and high speed performance are more important than accuracy. One example of such applications is DSP and Image Processing.

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