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Re-configuration and simulation of three-phase seven-level cascaded h-bridge multilevel inverter

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Abstract
Conventional cascaded multilevel inverter topologies exhibit a number of undesirable shortfalls such as low efficiency, increase in circuit complexity, high cost, high total harmonic distortion (THD) and high switching losses. This informed the basis of proposing a more reliable cascaded H-bridge multilevel inverter and reduced number of switches which is capable of mitigating these shortfalls. In this journal the number of switches was reduced from thirty six to eighteen and DC sources were reduced from nine to six to give the three-phase output power. The power circuit is tested using different switching control techniques namely alternate phase opposition disposition (APOD), phase disposition (PD) and phase opposition disposition (POD) as carrier signals. The results of the power quality measurements from the three switching control techniques were compared. From the simulation results, the least and highest THD was obtained at the modulation index of 1.0 and 0.2. Also the highest and lowest output voltage, current and power obtained for APOD, PD and POD carrier signal at modulation index of 1.0 and 0.2 respectively. The finding of this work established that as modulation index increases, the THD decreases and the values of the output voltage, current and power increases.

Keywords: cascaded H-bridge multilevel inverter, modulation control circuit

Introduction
Basically, inverter can be defined as an electrical devices that change direct current (dc) input voltage to a symmetrical alternating current (ac) output voltage of desired magnitude and frequency. The output voltage could be fixed or changeable at a fixed or changeable frequency. A changeable output voltage can be obtained by changing the input dc voltage and maintain the gain of the inverter (ratio of the ac output voltage to the dc input voltage) constant [4]. Conversely, if the dc input voltage is fixed and is not controllable, a changeable output voltage can be gotten by changing the gain of the inverter which is normally accompanied by pulse width modulator within the inverter [5]. The waveform of practical inverters are non-sinusoidal and contain some harmonics. Conventional inverter has some disadvantages, this are less efficiency, high cost and high switching losses. To overcome these disadvantages lead to its re-configuration and its modification [2]. Multilevel inverter begins with three levels converter and has been introduced since 1975. The cascade H-bridge multilevel inverters was first suggested in 1979 by Nabea [3]. In past years multilevel inverters (MLI) are used in high power and high voltage applications. Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform.

Conventional and Reduced Switches of Three-Phase Seven-Level Cascaded H-Bridge Multilevel Inverter
Research work that has gone on inverter circuit configuration especially in reducing the switches at higher voltage levels, by reducing switches and increasing voltage levels will reduce filter cost and harmonic content. Conventional three-phase seven-level cascaded H-bridge multilevel inverter topology required thirty six (36) switches and nine (9) separate dc sources, but to reduce switching loss and cost, Eighteen (18) switches and six (6) separate dc sources are required in which the same MLI output voltage are obtained [1]. Three-phase seven-level cascaded H-bridge multilevel inverter with reduced switches carried six switches in each phase. Each phase has two legs and carried three switches in each leg. The switches are named as S_1, S_2, S_3, to S_{18} and are arranged in first and second leg of each phase respectively as shown in Fig. 2 [7].

Asymmetrical Three-Phase Seven-Level Cascaded H-Bridge Multilevel Inverter

Asymmetric seven-level cascaded H-bridge multilevel inverter will be discussed in this journal because; The number of H-bridges, DC sources, THD and switching losses, will be reduce when compare with symmetric cascaded H-bridge multilevel inverter and as result of this, asymmetric cascaded H-bridge multilevel inverter has high speed capabilities and high conversion efficiency than symmetric cascaded H-bridge multilevel inverter [8]. Each level of asymmetric cascaded H-bridge multilevel inverter can generate seven different voltage levels, these are $+3V_{DC}$, $+2V_{DC}$, $+1V_{DC}$, $0V_{DC}$, $-3V_{DC}$, $-2V_{DC}$ and $-1V_{DC}$ by connecting the input DC voltage sources of $100^{V_{dc}}$ and $200^{V_{dc}}$ in each phase as shown in circuit Figure, 2 [1, 9]. The output voltage of a multilevel inverter is the sum of all the individual inverter outputs. Each of H-Bridge's active devices switches only at the fundamental frequency and generates a quasi-square waveform by level-shifting, it is positive and negative phase legs switching timings. Further, each switching device always conducts for 120^0 or 180^0 (or half cycle) regardless of the pulse width of the quasi square wave so that this switching method results in equalizing the current stress in each active device. This topology of inverter is suitable for high voltage and high power inversion because of its ability to synthesize waveforms with better harmonic spectrum and low switching frequency. The circuit diagrams of conventional three-phase seven-level cascaded H-bridge multilevel inverter is shown in figure 1 and reduced switches are shown in Figure 2 below

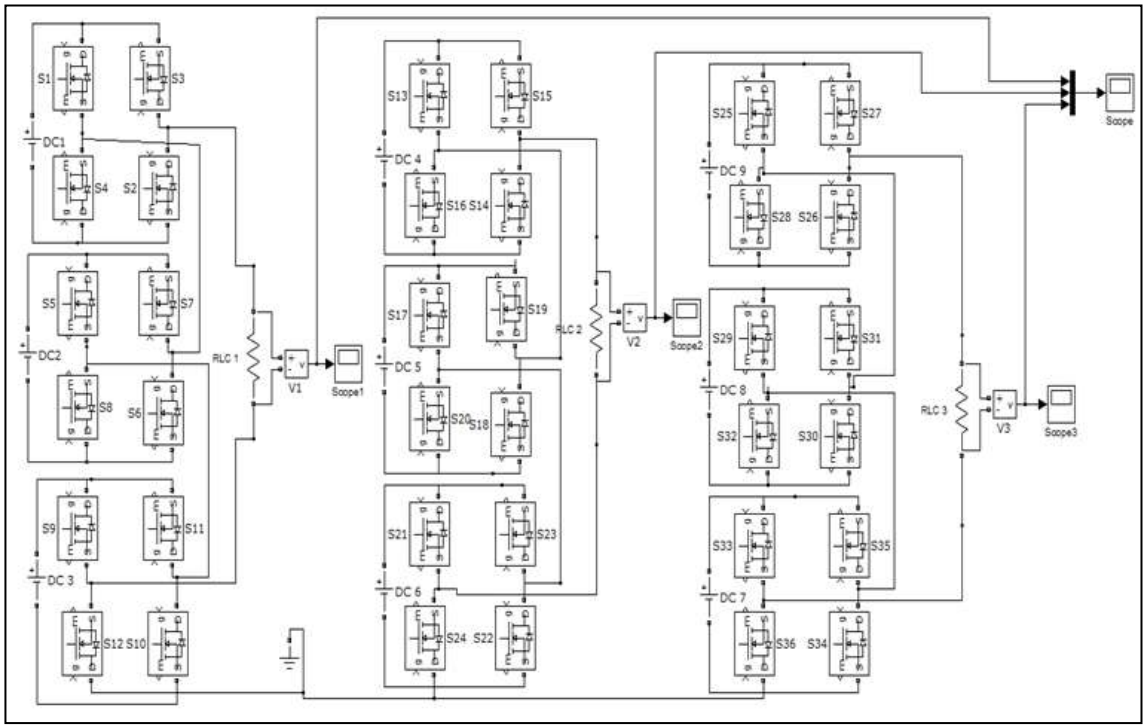

Fig 1: Circuit diagram of conventional asymmetric seven levels CHB MLI in MATLAB/SIMULINK.

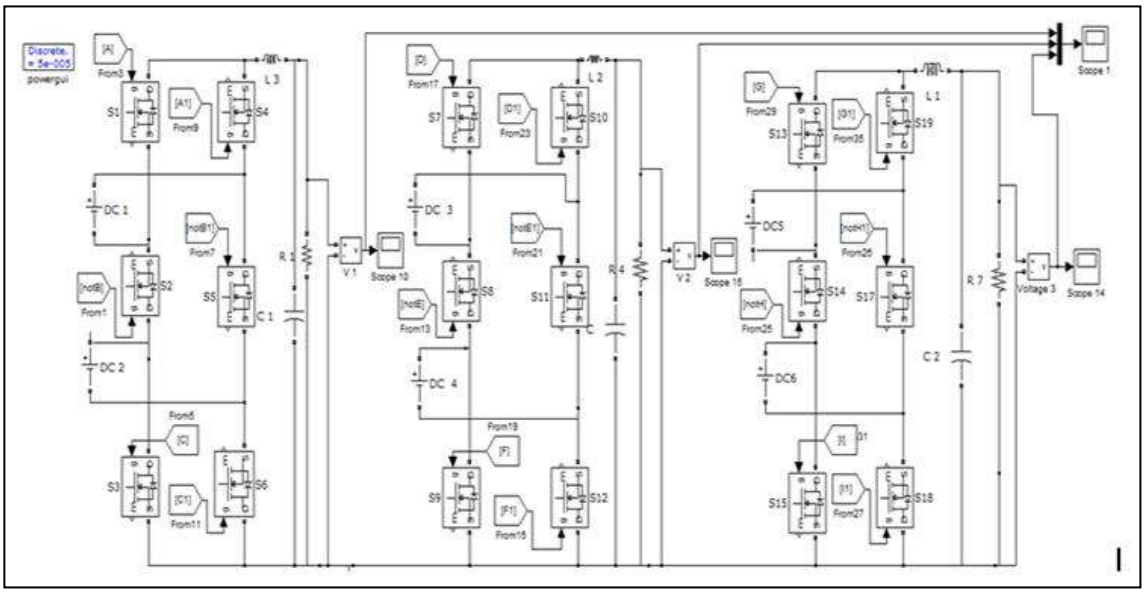

Fig 2: Circuit diagram 3-phase 7-level CHB MLI with reduced number of switches in MATLAB/SIMULINK

One of the disguising features of the above circuit is that it can be used as seven levels and five levels CHB MLI respectively, by making the two dc input voltages to be different (asymmetric) and make the two dc input voltage equal (symmetric). The three phase seven levels CHB MLI is basically an extension of the single-phase seven-level CHB MLI, except that the reference signal for different legs of three phase has a phase shift of 120^0 instead of 180^0 for the single phase [6]. This is illustrated in the Ac sine waveform in the figure below.

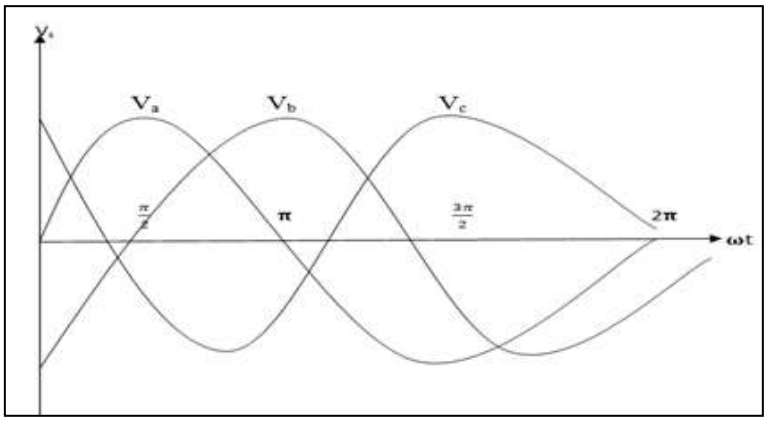

Fig 3: Ac sine wave of three phase asymmetric 7-levels CHB MLI

$V_a = V_m \text{Sin}\omega t + 0$, $V_b = V_m \text{Sin}\omega t + \frac{2\pi}{3}$ and $V_c = V_m \text{Sin}\omega t + \frac{4\pi}{3}$

$I_a = I_m \sin(\omega t - \phi)$, $I_b = I_m \sin(\omega t - \frac{2\pi}{3} - \phi)$ and $Ic = I_m \sin(\omega t + \frac{2\pi}{3} - \phi)$

The system is said to be balanced, because the voltages and curents have the same root mean aquare (RMS) and peak values in all phases and their phase angle are equal in space, hat is 120^0 symmetrical phase displacement [6]. Then total instantaneous power is given by

$P = V_aI_a + V_bI_b + V_cI_c$
$P = 3VI\sin\phi$.

Table 1: shown Switching States of Single-phase Asymmetric Seven-level Cascaded H-bridge Multilevel Inverter with Reduced Number of Switches

S/n	Switching Sequences						Voltage levels
	S_1	S_2	S_3	S_4	S_5	S_6	
1	0	1	0	1	0	1	$+3V_{dc}$
2	1	1	0	0	0	1	$+2V_{dc}$
3	0	1	1	1	0	0	$+1V_{dc}$
4	0	0	0	1	1	1	$0V_{dc}$
5	1	0	0	0	1	1	$-1V_{dc}$
6	0	0	1	1	1	0	$-2V_{dc}$
7	1	0	1	0	1	0	$3V_{dc}$

Modulation control signal

Figure 4, 5 and 6 shows the modulation control circuit for a phase opposition disposition (POD), phase disposition (PD) and alternate phase opposition disposition (APOD) respectively. These control circuits generate pulses that control the switching pattern of N-channel MOSFET switches in the H-bridges. This was configured based on their repeating sequence.

Repeating Sequence

The repeating sequence generates arbitrary shape of periodic signals and is made up of a time value and an output value in the circuit.

The Time Value

The time value was designed based on a chosen switching frequency of 5 kHz. Which was configured as [0 (1/(2*5000)) (1/(5000))] in Simulink of the chosen MATLAB version.

The Output Value

The output value depends on how the waveform should be specified. And this is based on the type of carrier disposition that will be chosen for a preferred implementation [1]. The configuration of the carrier signals in Simulink is as follows.

S/n	APOD	PD	POD
3	2 3 2	2 3 2	2 3 2
2	2 1 2	1 2 1	1 2 1
1	0 1 0	0 1 0	0 1 0
-1	0 -1 0	-1 0 -1	0 -1 0
-2	-2 -1 -2	-2 -1 -2	-1 -2 -1
-3	-2 -3 -2	-3 -2 -3	-2 -3 -2

For example, Figure 4 was configured based on POD carrier signal and the signal are arranged in a symmetric mirror image above and below the zero reference axis, Figure 5 was configured based on PD carrier signal and the signal are arranged in the same direction, Figure 6 was configured based on APOD carrier signal and the signal are arranged in the same direction, but the neighborhood carrier signal are in the opposite direction.

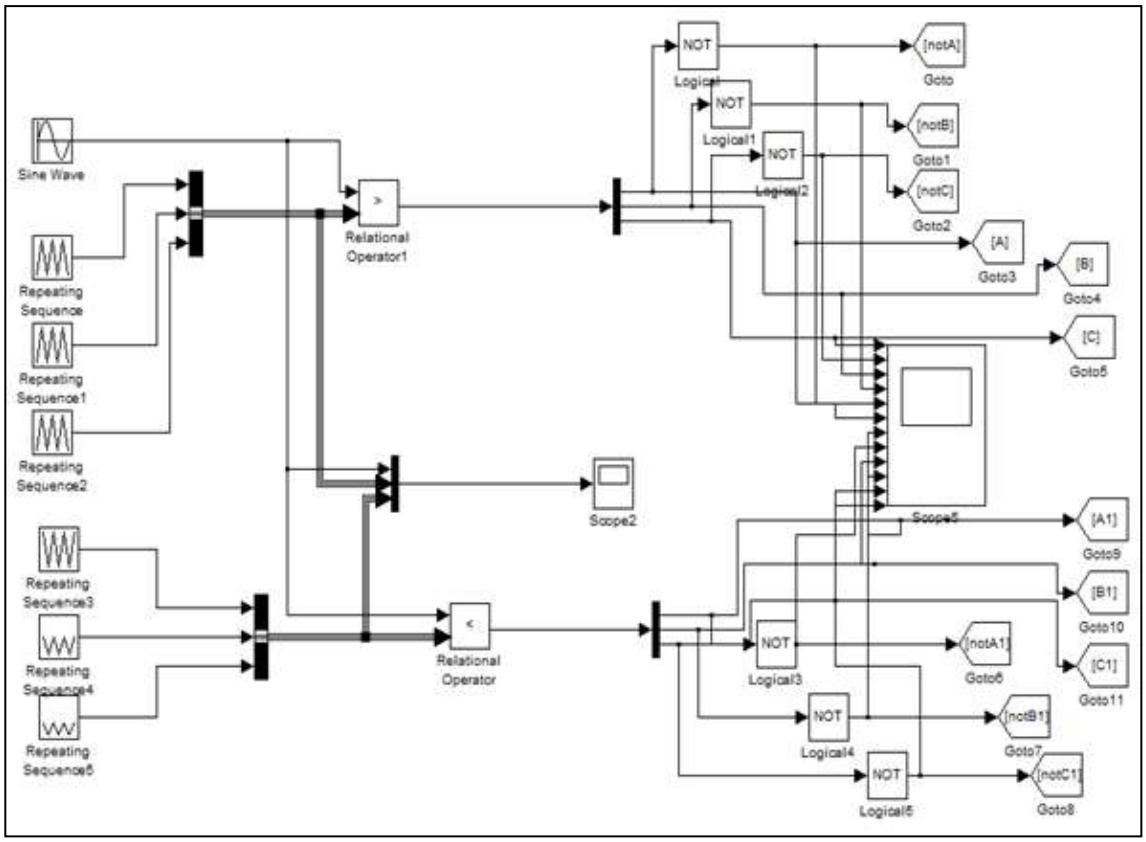

Fig 4: Modulation control circuit using POD carrier signal

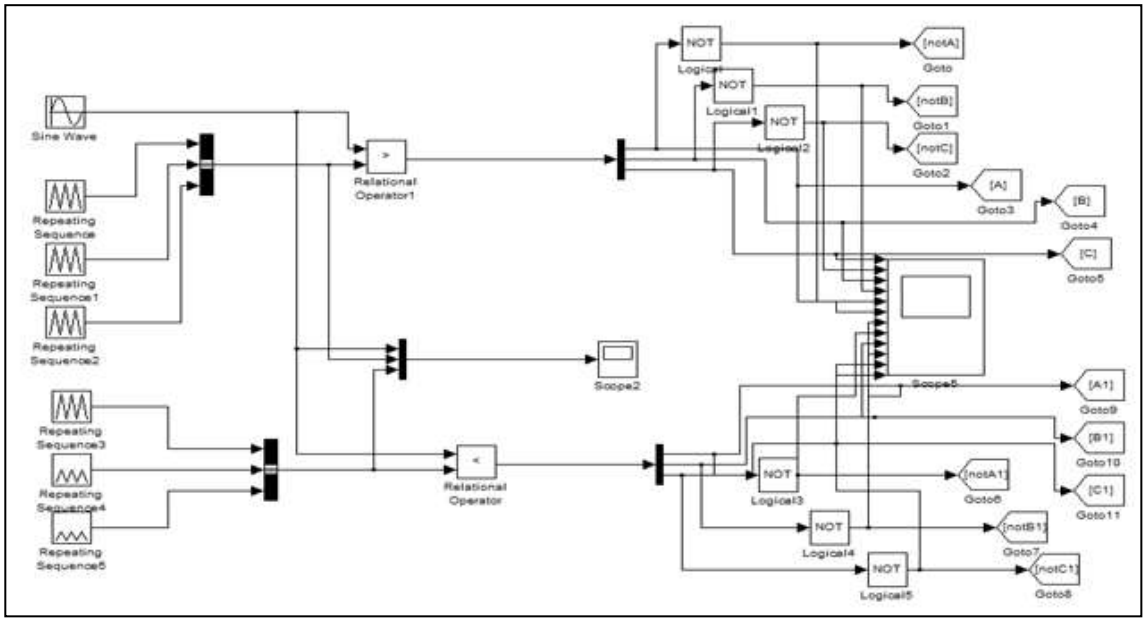

Fig 5: Modulation control circuit using PD carrier signal

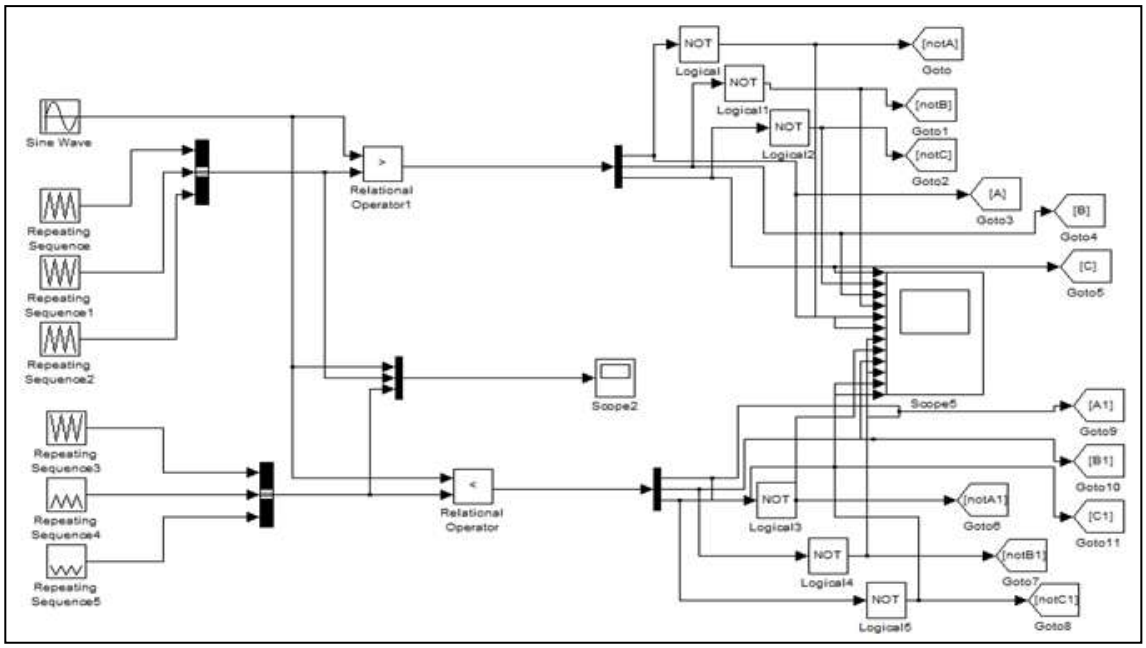

Fig 6: Was configured based on APOD carrier signal respectively.

Simulation output waveforms of cascaded H-bridge multilevel inverter in MATLAB/SIMULINK

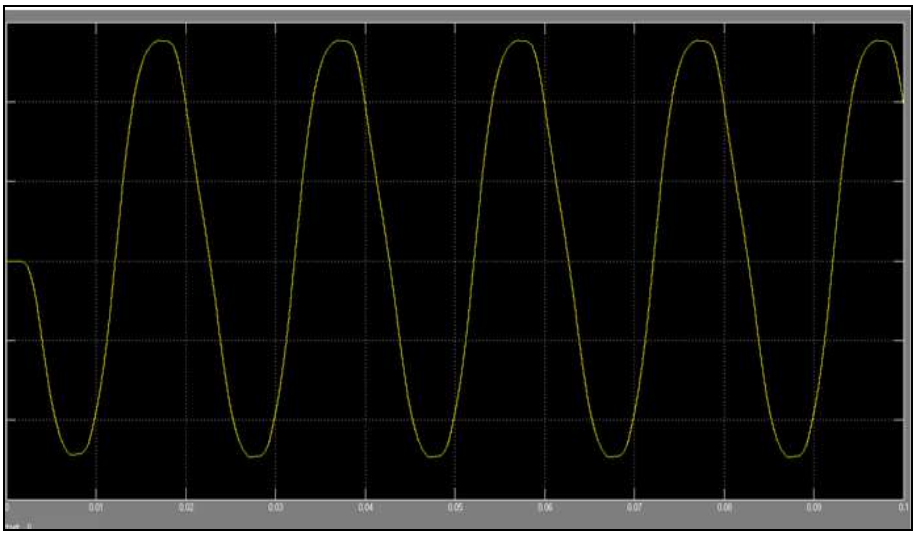

Fig 7: Output voltage waveforms of a filtered single-phase seven-level asymmetric CHB MLI

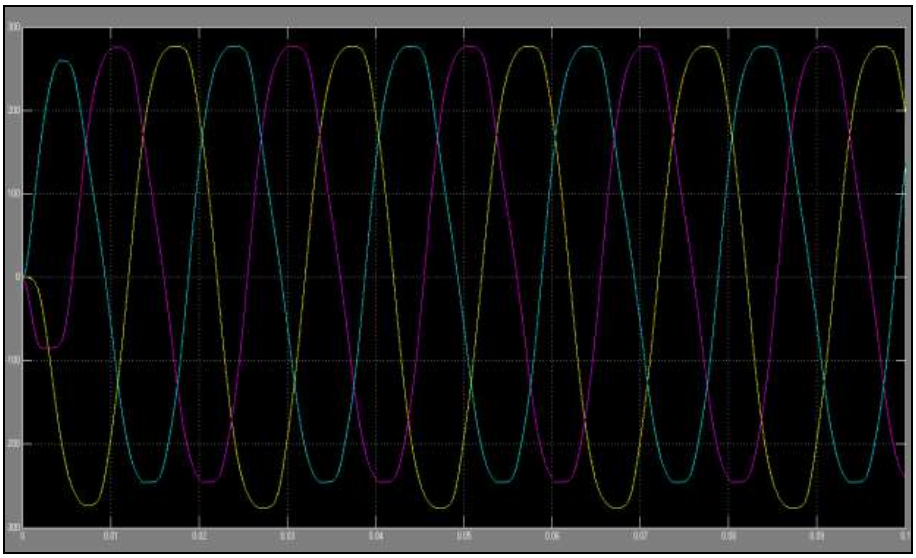

Fig 8: Output voltage waveforms of a filtered three-phase seven-level cascaded H-bridge multilevel inverte

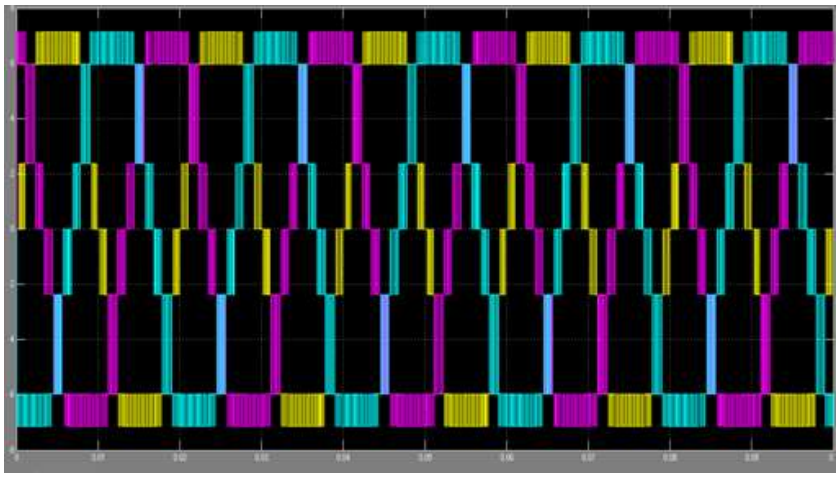

Fig 9: Output waveform of three phase 7-levels asymmetric CHB MLI

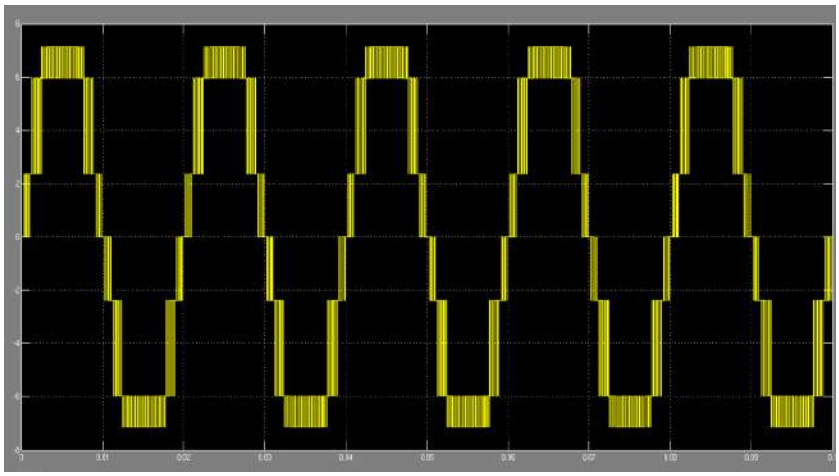

Fig 10: Line to ground output voltage waveforms of single-phase seven-level Cascaded H-bridge multilevel inverter (CHB MLI)

Results

All these results were obtained during the simulation of reduced switches of cascaded H-bridge multilevel inverter circuit in Figure 2 in MATLAB/SIMULINK, from modulation index of 0.2 to 1.0

Table 2: THD, Output Voltages. Output Current and Output Power of Single-Phase Seven-level Cascaded H-bridge Multilevel Inverter using APOD Carrier Signal obtained during Simulation in MATLAB/SIMULINK.

S/n	Modulation Index	THD (%)	Output Voltage(V)	Output Current(A)	Output Power(W)
1	0.2	76.98	29.45	0.29	8.67
2	0.3	72.08	39.41	0.39	15.53
3	0.4	75.28	99.70	1.00	99.40
1	0.5	63.75	102.90	1.03	105.88
S	0.6	44.33	181.30	1.81	328.70
6	0.7	36.49	222.30	2.22	494.17
7	0.8	31.99	239.10	2.39	571.69
8	0.9	24.48	268.70	2.69	722.00
9	1.0	22.22	277.30	2.77	768.95

Table 3: Shown THD, Output Voltages, Output Current and Output Power of Single-Phase-Seven-level Cascaded H-bridge Multilevel Inverter using PD carrier Signal obtained during Simulation in MATLAB/SIMULINIC

S/N	Modulation THD(%) index		Output voltage(V)	Output Current(A)	Output Power(W)
1	0.2	79.58	28.07	0.28	.88
2	0.3	74.74	38.21	0.38	14.60
3	0.4	73.70	100.00	1.00	100.00
4	0.5	63.72	103.30	1.03	106.71
5	0.6	44.29	181.40	1.81	329.06
6	0.7	36.16	223.60	224	499.97
7	0.8	31.92	238.90	2.39	570.73
8	0.9	24.20	268.60	2.69	721.46
9	1.0	22.10	277.10	2.77	767.84

Table 4: Shown THD. Output Voltages. Output Current and Output Power of Single-Phase Seven-level Cascaded H-bridge Multilevel inverter using POD Carrier Signal obtained during Simulation in MATLABISIMULINK.

S/N	Modulation Index	THD (%)	Output Voltage(V)	Output Current(A)	Output Power(M)
1	0.2	76.98	29.45	0.29	8.67
2	0.3	72.08	39.40	0.39	15.5[1]
3	0.4	'·4.57	100.10	1.00	100.10
4	0.5	63.19	103.10	1.03	106.30
5	0.6	44.4-	181.70	1.82	330.15
6	02	36.39	223.70	2.24	500.42
7	0.8	32.14	238.90	2.39	570.73
8	0.9	24.32	268.80	2.69	722.53
9	1.0	22.09	277.00	2.77	767.29

Conclusion

The prime advantage of using multilevel inverters in implementing power supply circuits is to reduce the harmonics distortion and switching losses in the power circuit. In addition, power is distributed across many switching components hence reducing failure rate of components and allows for high voltage to pass through it. For the purpose of reduction in the overall cost of implementing the power circuit, the number of switches was reduced to eighteen instead of thirty six switches that is associated with the conventional cascaded H-bridge multilevel inverter. MATLAB/SIMULINK simulation package was used to obtain the Fast Fourier analysis of the power circuit been switched by APOD, PD and POD sinusoidal PWM at varying values of modulation index.

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