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Comparative analysis of low power 8T SRAM

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Abstract
There is requirement for a higher noise tolerant and low power static random access memory (SRAM) in today's market. A stable 8 transistors SRAM (8T SRAM) cell is presented in this paper for low power operation. The presented SRAM cell has a structure similar to standard 6 transistors SRAM (6T SRAM) with additional 2 buffer transistors and a complementary word line. Additional buffer transistors are added to ensure low leakage power due to stacking effect. Parametric comparison with standard 6T SRAM is done in this paper. Design metrics such as read static noise margin (RSNM), write trip voltage (WTV) and leakage power are compared. The proposed cell dropped leakage power 85% of the standard 6T SRAM cell.

Keywords: Low power, read static noise margin (RSNM), sensitivity, static random access memory (SRAM), write trip voltage (*WTV*), N-curve, 45nm.

1. Introduction
Static random access memory (SRAM) was invented in 1963 by Robert H. Norman at Fairchild Semiconductor which led to the development of complementary metal oxide semiconductor (CMOS) SRAM in 1964 by John Schmidt. It was a high performance, power efficient and cheaper alternative for magnetic core memory. Production of MOS memory chips was enabled by Federico Faggin's MOS IC. Today SRAM is used as virtual memory, RAM disk and Shadow RAM along with its use as cache memory to provide temporary storage for operating system (OS) and applications.
In comparison to dynamic random access memory (DRAM), SRAM is faster but is more expensive. Basic difference between the working principle of SRAM and DRAM is that SRAM does not require periodic refresh of data whereas DRAM does require periodic refresh of data. With the development in technology, processors are becoming faster but they are being limited by slower speeds of RAM, to overcome this issue SRAM is used as cache memory which is an interface between DRAM and processor to provide faster data acquisition.

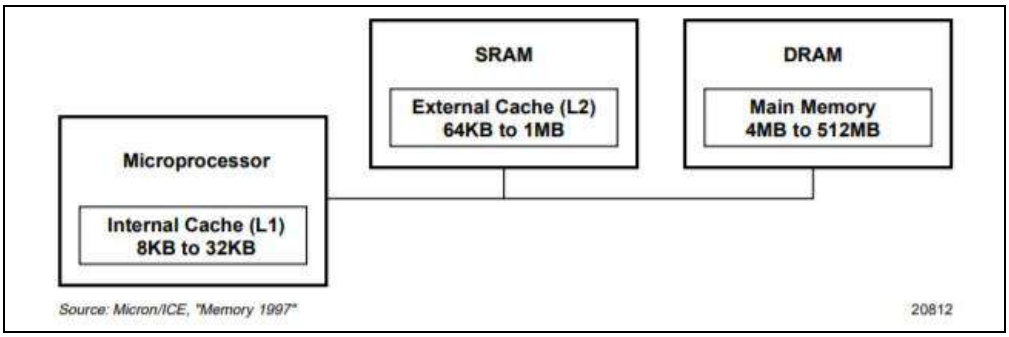

Fig 1: SRAM used for interfacing between DRAM and Microprocessor

With an increase in demand for mobile devices, high-performance efficient devices are needed. SRAM also overcomes this problem as SRAM is more power efficient than DRAM. Some implementations for low powered SRAM limit the performance of SRAM but they still manage to provide equal access time as DRAM which has lower power consumption than SRAM.
To fulfil the emerging need of high performance computing system on chip (SOC), a SRAM architecture with low power consumption and high performance parameters (i.e. read static

noise margin (RSNM), read access time (TRA), and write access time (TWA) [2] is required.

Data stored in SRAM does not require any periodic refresh till sufficient power is supplied to it. Most commonly used SRAM topology is 6T SRAM which is a full CMOS SRAM design. Using CMOS design helps with better noise margins and switching speed, but it is bulkier and less cost efficient. Below are some advantages and disadvantages of SRAM:

- SRAM have symmetrical Read/Write cycle i.e. Read time is equal to write time.
- There is no structural stress while using SRAM IC i.e. it has an infinite endurance.
- There is availability of multiple vendors of SRAM which result in a good variety of products i.e. higher possibility of availability of SRAM with desired parameters in the bulk market.
- A separate power source (battery) is required to hold up power as it loses data on power disruption.

Transistor stacking technique has been implemented for the low power application of 8T SRAM. The presented cell has a structure similar to a conventional 6T SRAM cell with two buffer transistors added along with a complimentary word line. With implementation of stacking effect, the presented cell achieves lower power dissipation as it limits sub-threshold leakage current.

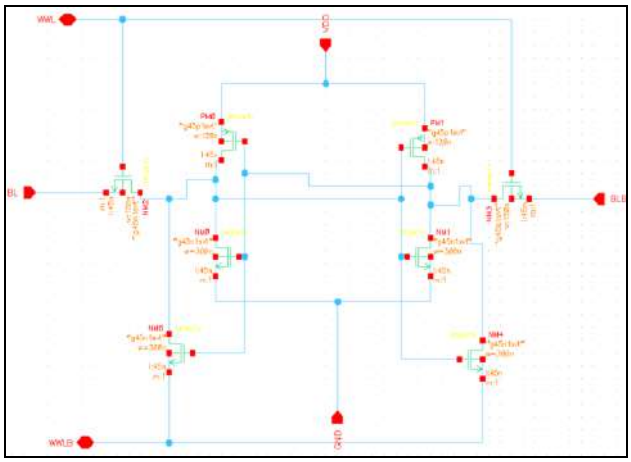

Fig 2: Proposed Low Power 8T SRAM cell.

Transistor static technique is implemented in proposed design as shown in Fig. 2. It is useful to limit sub-threshold leakage current. The sub-threshold current that flows through a stack of transistors that are connected in series reduces as two or more transistors in the stack are turned off. This effect of the reduction of static current is known as the "stacking effect" or "self-reverse bias" [7]. Voltage induces an exponential effect on leakage current in both i.e. NMOS and PMOS transistors. VG is "0" thus increasing VS reduces leakage current exponentially for NMOS in sub-threshold condition.

In this paper, a low-power, high stability CMOS 8T SRAM cell for low power applications is proposed. This paper can be summarized as below.

1) The cell proposed uses CMOS differential structure which improves sense margin.
2) Better read stability is obtained using the proposed cell.
3) The Low power 8T SRAM have lower leakage current when compared to standard 8T SRAM at 45 nm technology node

In Section II, operation to read, write, and hold of low power 8T SRAM are described. In Section III, the simulation results are discussed. Finally, in Section IV the paper is concluded.

2. Proposed LP8T cell

It can be observed that the above 8T SRAM cell is same as the conventional 6T which is a differential SRAM but this presented design has two extra buffer transistors (MN4/6) and a complimentary word line (WWLB). Benefit of using the buffer transistor is that during a read operation either of the buffer transistors conducts to help achieve better read time which also improves read stability of the design. It is known that number of junction and leakage current are directly proportional to each other which lead to increase in leakage current during hold operation of the SRAM.

Another important aspect to achieve lower leakage current and higher performance is transistor sizing. In every SRAM it has been observed that there is a trade-off between read SNM and write SNM of the SRAM. βratio i.e. pull up ratio of the SRAM is considered to deliver best performance between 1.2 and 3 whereas pull-down ratio (PR) is consider to deliver best performance when it is as low as possible as generally it is taken as 1 i.e. to ensure that write operation is carried out successfully.

For fair comparison this configuration is used in both 6T SRAM and 8T SRAM.

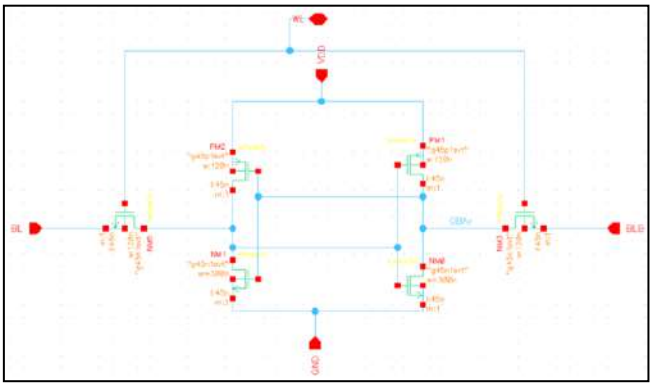

Fig 3: Standard 6T SRAM cell (D6T).

The various modes of operation of LP8T SRAM are discussed below.

A. Read Operation

To achieve a successful read operation, both the bitlines of the SRAM are pre charged to VDD along with the wordline of the SRAM whereas the complementary wordline is lower to zero by connecting to ground level. According to the stored data either of buffer transistors conducts. Current is conducted through access transistors and sense amplifier senses the difference in voltage to provide a valid output. Buffer transistors help to achieve results faster and decrease the read time.

B. Write Operation

To achieve a successful write operation the wordline of the SRAM is pre-charged to VDD whereas the complementary wordline is lower to zero by connecting to ground level. Because the wordline is high both access transistors of the SRAM are turned ON. If node H of the SRAM has logic 1 stored in it initially and node L has logic stored in it now if

we store logic 1 to node L and logic 0 to node H then access transistor corresponding to node H discharges the node and other access transistor pre charges node L to VDD. This whole procedure ensures a successful write operation.

C. Hold Operation

In order to achieve a successful hold operation access transistors are turned OFF because wordline is connected ground whereas complementary wordline is connected to VDD. Leakage current is directly proportional to the number of junctions in SRAM cells.

3. Simulation Results

This section presents simulation results and discussions based on the simulation setup provided below.

A. Simulation Setup

With the help of Cadence Virtuoso IC design tool 45 nm technology node is implemented in this design. Minimal voltage for 45 nm technology node is 1.1 V hence, simulation results are recorded for voltage varying from 1.1 V to 1.5 V. To ensure robust SRAM design and obtain high SNM and read current β ratio should be between 1.25 and 2.5 and hence, simulation results are recorded for β ratio varying from 1.25 to 2.5 to observe the effect of β ratio on SNM using N curve. Various setups are required for different simulations which will be discussed further.

B. Read Static Noise Margin (RSNM)

RSNM is the most useful measure for quantifying how stable a SRAM is during the read cycle as well as for hold state. Static Noise Margin (SNM) is the highest value of noise generated by a DC source which does not change the stored data in the inverter pair in other words the highest value of DC noise till which the cell retains its data [45]. RSNM is also known as readability of a SRAM as well as read stability of the SRAM as it gives a measure about stability of the read process of a SRAM. The SNM for read operation is obtained through the voltage transfer characteristics (VTC) for operation of reading of the SRAM. To obtain read VTC sweep the voltage of the data nodes i.e. node H or node L with BL and BLB (i.e. both bitlines) and WL (wordline) at VDD while the node voltage is monitored at other nodes.

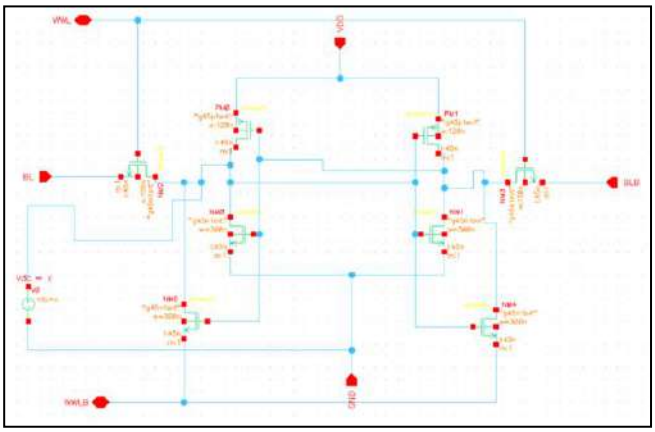

Fig 4: Design of 8T SRAM bitcell displaying the worst case polarity noise

Increase in V_N results in change in cell's stability. Stability during reading operation is more significant than during the hold operation. SNM is severely degraded by increase in V_N and it is determined by β ratio i.e. bitcell ratio. As shown in above figures, to model the SNM worst case polarity is included.

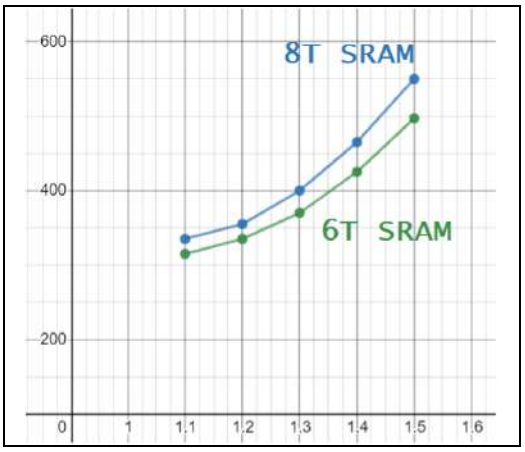

Fig 5: SNM for 6T and 8T SRAM at various VDD

C. Leakage power

Leakage power is a measure of power when the SRAM is hold state. Leakage power effects data retention duration of a SRAM. If the leakage power is high then SRAM will not be able to retain data for a longer time as the stored charge will leak through it much faster compared to a low leakage power SRAM.

To have a SRAM in hold state both the bitlines must be precharged to VDD and wordline must be connected to GND and complementary bit lines are connected to VDD.

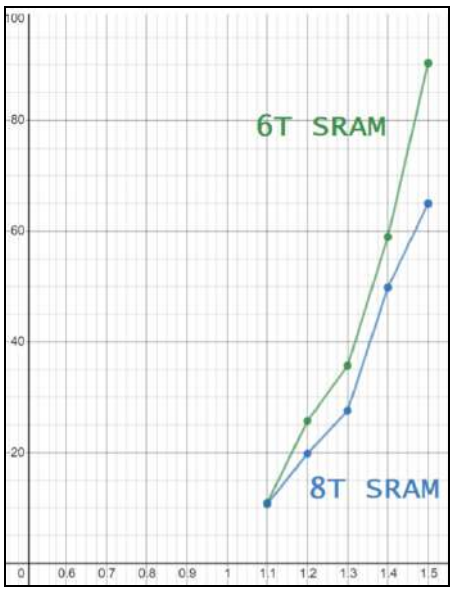

Fig 6: Leakage power analysis for 6T and 8T SRAM at various V_{DD}

D. N-curve

As already discussed, SNM is the best measure for the purpose of quantification of the stability of SRAM because SNM is the largest DC noise which can be allowed without altering the charge at internal nodes in other words to flip the charge. We can use Hold SNM, write trip voltage and read SNM for analysis of performance and design of SRAM but none of these has the information about current flow data which has an extreme significance.

The disadvantages of SNM obtained by using butterfly curves are below:

- The delimitation of the voltage transfer characteristic (VTC) which is generated using the butterfly curve. It is delimited to a maximum of 0.5VDD.
- SNM is calculated from the data obtained. Therefore, it is not possible to measure SNM by automatic inline tester.
- As SNM is available indirectly, it is not possible to create information for failures of SRAM.
- For read and write measurement different analysis are needed.
- It doesn't have any information about current flow which is an important metric for analysis of SRAM stability.

To satisfy the above requirement i.e. to overcome these disadvantages N-curve can be used for an SRAM design. Same setup as used for measuring SNM using butterfly curve is used to obtain N-curve. Here the current through noise source represents Iin and voltage at the internal node connected to noise source is represented as V_{in}. N-curve is the I_{in} v/s V_{in} plot for this setup.

N-curve analysis simplifies the calculation of read and write SNM and enables evaluation more accurately. Below is the metric evaluated using N-curve:

- The static voltage noise margin (SVNM):

SVNM in easy words can be explained as the difference in voltage between two points, say point A and point B. This difference represents the maximum tolerance of noise by DC source of an SRAM at the input before the contents of SRAM are changed

- The static current noise margin (SINM):

The maximum value of the direct current that can be inputted to an SRAM before it will change its stored content is known as SINM. In N-curve, it is given by the maximum values of Iin between points, A and B.

- The write trip voltage (WTV):

This performance metric of SRAM concerns the writing ability of the SRAM. It is defined as a voltage drop that is required to alter logic 1 stored in SRAM internal nodes to logic 0 and vice versa. In N-curve, it is given by the difference between points, B and C.

- The write trip current (WTI):

The minimum amount of current required to write to the SRAM given that it's both bitlines are precharged to VDD. In N-curve, it is the maximum negative values of Iin between point A and point B.

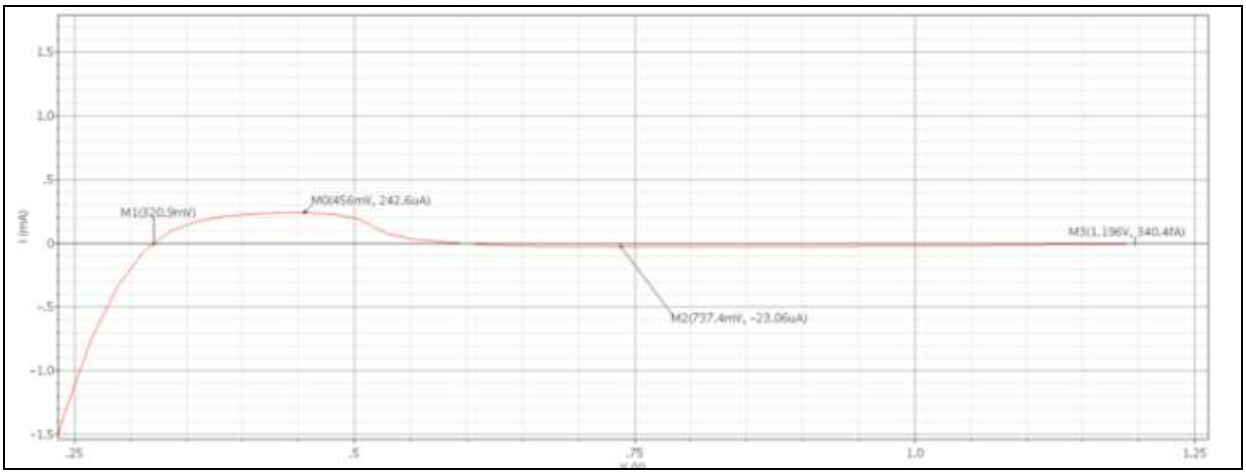

Fig 7: N-curve analysis for 8T SRAM at V_{DD}=1.2 V

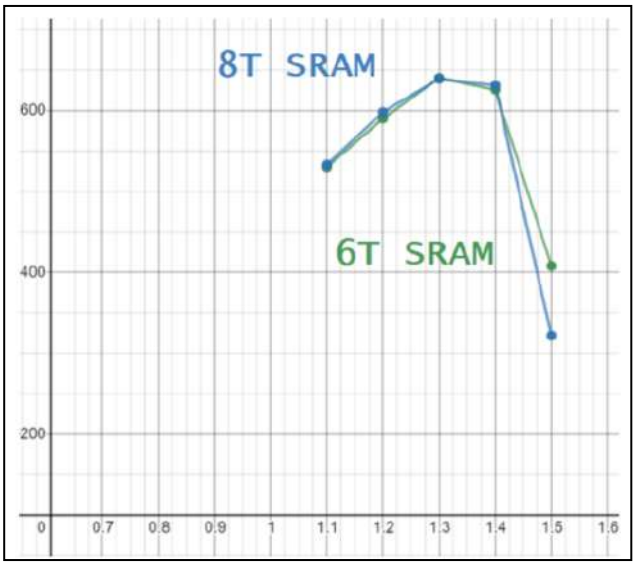

Fig 8: WTV analysis for 6T and 8T SRAM at various V_{DD}

Table 1: Performance Comparison among Low Power 8T and standard 6T SRAM

	Standard 6T SRAM			Presented 8T SRAM		
V_{DD} (V)	SVNM (mV)	WTV (mV)	Leakage power (µW)	SINM (mV)	WTI (mV)	Leakage power (µW)
1.1	317	523	10.8	341	526	10.3
1.2	334	582	25.7	352	597	19.8
1.3	371	624	36.3	403	633	27.3
1.4	423	608	58.6	462	617	49.2
1.5	504	407	90.4	557	362	64.7

4. Conclusion

In this work, 8T SRAM design is implemented using Cadence Virtuoso. The outcome of this work that is properly working as per our requirement. The power

consumption is lowered up to 83% of standard 6T SRAM. It can also be observed that faster read operation and lower leakage current have been obtained. Hence, it ensures better data retention for a longer period of time. In this work 8T SRAM uses stacking effects to lower the leakage current in low power applications.

We have presented various simulation results which verify that the objective of this dissertation work is obtained i.e. a robust SRAM design is obtained with improved SNM, better read speed and better data retention.

The present work provides a powerful, low-power consuming, large noise tolerant 8T SRAM cell. We present analysis of various parameters like access delay, stability of reading operation, hold power, etc. We observe better performance in terms of most of the parameters analysed, in comparison to the other cells. Thus, the proposed cell is a better choice for low power, high-noise tolerant SRAM cells in scaled technology.

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