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Design and construction of a digital clock with hourly alarm

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Abstract

Clocks are devices used to measure the passage of time. The clock was generated using logical gates instead of crystal oscillator which is more stable, but due to its cost and unavailability was not in the implementation of this project. The frequency obtained from the time base was exactly a clock signal of 1Hz, which was used to drive the circuit. The main circuit of clock was implemented counter and decoder instead of microprocessor used in conventional digital clocks. Due to the size and nature of components used the project could not be made smaller than the clocks that are factory made. Clocks require a source of power and means of transmitting and controlling it, as well as indicator to register the lapses of time. It also contains an alarm circuit that send out an alarm signal on hourly basis.

Keywords: Counter, decoder, seven segment display, comparator

Introduction

Electronic designers have measurable significance on digital devices since late 1960s, this is due primarily to rehabilitee and improved accuracy gained when using electronics device in two level mode (binary mode) as compared to using electronic devices in a continuous mode (analog mode). As silicon integrated circuit (ICS) become denser and none consistently reproducible over past few decades, so did digital electronics devices. Today digital circuit and digital systems produced from digital device can be found in every work of life ranging from children's toys, kitchen appliances, laboratory instruments, office instruments, advertisement industry, personal and workstations and computers to space satellite application. Clock, which is a device for indicating the passage of time, has been in existence over the year which ranges from the glass to the sundial and the controlled clocks. Most clocks contain means of producing a regular recurring action such as the swing of a pendulum, the oscillation of a spinal on the balance wheel. The recurring action of a mechanical clock depends on the swing of the pendulum, the oscillation of a balance wheel and balance spring. Digital clock with hourly alarm is one means of measuring time electronically; this means been unique has various advantages that go along with it usage. Being electronic, it can be manipulated to any degree based on the designers choice and could be used in virtually every aspect of the society that needs to schedule the time for its activities.

The Design

In this section the design of the various unit of the system built up, the theory of the device used and their operation were considered. The design is based on the availability of the components for the system realization. The various units were designed and tested separately. This includes the power supply unit. Time base, counters, display unit and alarm circuit.

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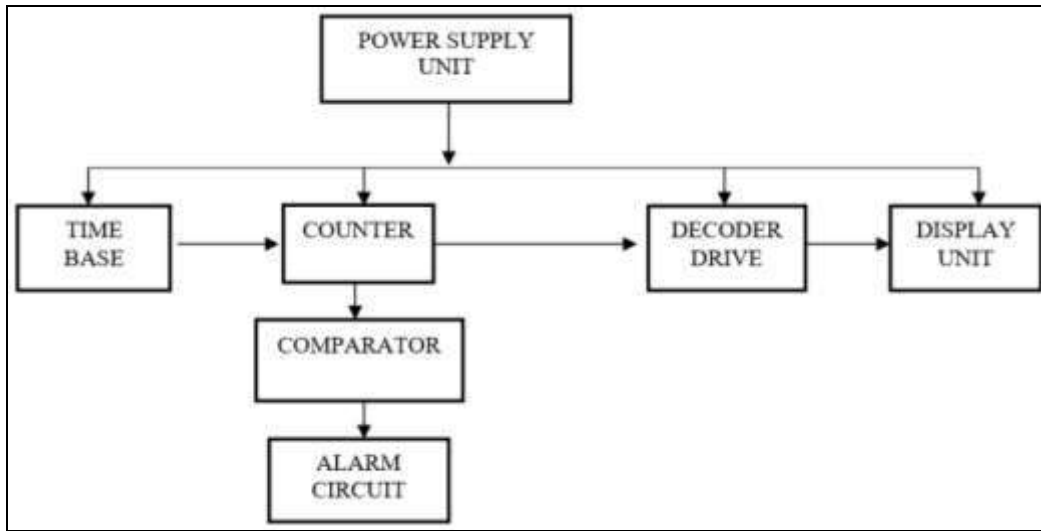


Fig 1: Block Diagram of Digital clock with hourly alarm

Power Supply Unit

The main function of power supply unit is to supply power to every functional block in the system for their effective operation. This comprises of a major unit in all electronic circuits and is required to power the entire unit in the system

at a stable dc voltage. This unit is designed to produce a +5v dc output at a specified maximum current from an existing ac main source. Figure 1below show the block diagram of power supply unit.

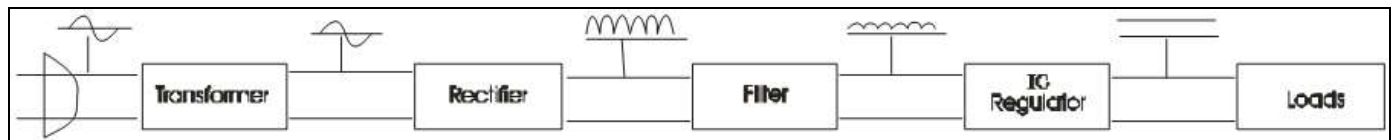


Fig 2: Block Diagram of Power Supply Unit

Design Requirements for Power Supply Unit

1. Conversion of input AC mains power to DC
2. Provision of a regulated +5V supply output

Components Required

1. A transformer (step-down)240V-12V (50Hz)
2. Rectifier diode
3. Filtering capacitor
4. Voltage regulator
5. Resistance of limiting resistor to power indicator

Transformer

This is a step down transformer, which step down 240V main ac to 12V dc. Therefore 240/12V transformer rating is used. The system voltage requirement is 5V.

The system input resistance is about 200Ω . Therefore, the expected load current is

$$I \equiv \frac{V}{R}$$

Where

- I ≡ Load current of the power supply
- V = Voltage requirement for the entire circuit
- R = Input resistance of the power supply.

$$\text{Therefore } I = \frac{V}{R} = \frac{5}{200} = 250mA$$

A transformer with current rating of 500mA which is greater than load current was used. Thus power rating of the

transformer was computed to be

$$S = VI$$

Where S = power rating of the transformer
 I = current rating of the transformer
 V = Voltage of the transformer

$$\text{Therefore } S = IV = 12 \times 0.5 = 6V$$

Rectifier

This is the part that carries out rectification by converting alternating current (a.c) voltage to steady direct current (d.c) voltage. The voltage employed a bridge rectifier arrangement. The circuit diagram is shown below.

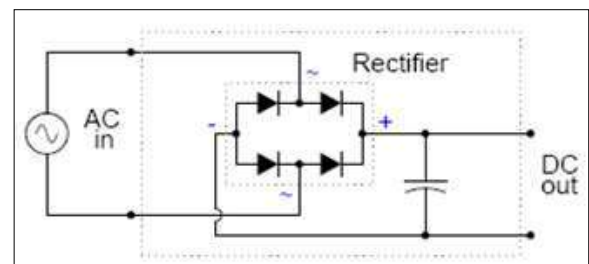


Fig 2.4: Full wave bridge rectifiers

Filter

This is the part that smoothed out ripple from rectified waveform in order to generate pure d.c. this is achieved by the use of a filter capacitor (electrolytic) connected with its appropriate terminal across the rectified output.

Filter Capacitor Design

$$C_f = \frac{dt}{dv} IM$$

Where C_f = filtering capacitor
 dt = time between peak of the input waveform.
 I_m = peak current of load current
 dv = ripple voltage of the rectifier
 $dt = 1/2f$

Where f = frequency of the supply voltage = 50Hz

$$dt = \frac{1}{2 \times 50} = 0.01$$

$$dv = \delta_f V_{dc}$$

Where δ_f = ripple factor for full wave rectification

$\delta_f = 0.482$ from data book

V_{dc} = average input unregulated dc voltage for LM 7805 regulator

V_i = minimum input voltage for LM 7805

$V_i = 7.3V$ from data book.

$V_{dc} = V_i + V_D$

Where V_D is the voltage drop across LM 7805 and is 2V from data book.

Therefore $V_{dc} = 7.3 + 2 = 9.3V$

Therefore $dv = \delta_f V_{dc} = 0.482 \times 9.3 = 4.483V$

$$I_m = I_{rms} \sqrt{2}$$

Where I_{rms} = root mean square current

$I_{rms} = 0.5A$ from data book.

$$I_m = 0.5 \sqrt{2} = 0.7071A$$

Therefore filtering capacitor now will be

$$C_f = \frac{dt}{dv} I_m = \frac{0.01}{4.483} \times \frac{0.7071}{1} = 1577 \mu F$$

But standard capacitor values are 1000 μF and 470 μF .

Resistance of limiting resistor to power indicator (Reference to power supply Circuit)

$$R_{LED} = \frac{V_{cc} - V_f}{I_f}$$

Where V_{cc} = Regulated output voltage

V_f = LED forward voltage

I_f = LED forward continuous current

$$R_{LED} = \frac{(5 - 3)}{10mA} = \frac{2}{10 \times 10^{-3}} = \frac{2}{10^{-2}}$$

$$= 2000\Omega$$

Voltage Regulator

The regulator is a single chip that regulates the ripple free rectified voltage to give a constant output voltage regardless of the loading conditions applied in the main circuit. The LM 7805 voltage regulator IC with a +5V dc output were utilized in this project.

The complete circuit diagram of the power supply unit is shown in the figure below:

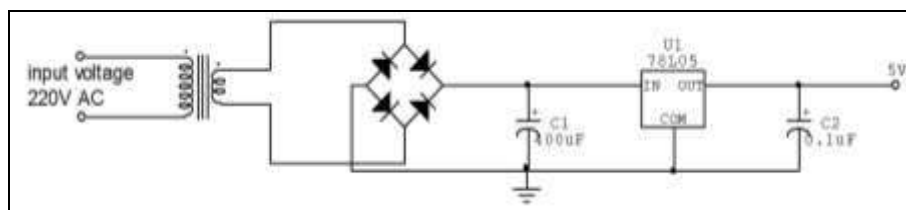


Fig 2.15: Power Supply Unit Diagram

Seven--segment Display Design (Common – Anode)

Design of limiting resistance of the resistor R

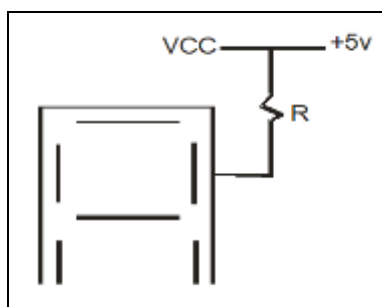


Fig 3: Common –Anode seven-segment Display

$$R = \frac{V_{cc} - V_{ol}}{I_{ol}}$$

Where V_{ol} is output low voltage

I_{ol} is output low current

$V_{ol} = 0.5v$ from Data sheet

$I_{ol} = 8mA$ from Data sheet.

$$R = \frac{5 - 0.5}{8 \times 10^{-3}} = 562.5\Omega$$

Alarm Circuit Design

Astable Mode of Operation

Design of 555 Timer IC driving on NPN transistor and LED

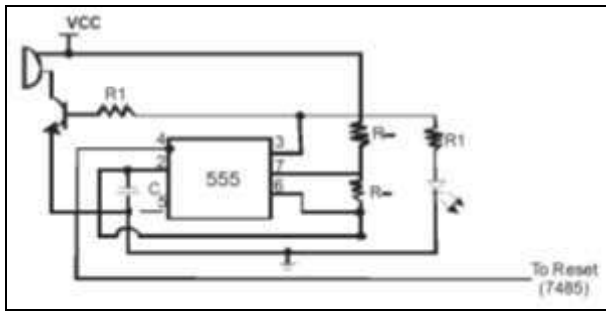


Fig 4: Astable 555 Timer IC

Frequency of 1 KHz was required to be generated by 555 timers

I choose $R_A = 1k\Omega$ and $R_B = 100k\Omega$

$$C = \frac{1.44}{R_A + 2R_B} = \frac{1.44}{(1 + 2 \times 100)10^{-3}} = \frac{1.44}{201 \times 10^3}$$

$$= 7.16 \mu F$$

Standard capacitor value from datasheet = $10 \mu F$
Output high voltage level of 555 timer (V_{OH})

$V_{OH} = 4.8v$ (from Data sheet)

$$R_2 = \frac{V_{OH} - V_f}{I_f}$$

Where V_f = Led forward voltage
 I_f = Led forward current

$$R_2 = \frac{4.8 - 2.2}{10mA} = 2600 \Omega$$

But standard resistor value = 2700Ω

Transistor $V_{BE} = 0.5v$ (2N4123)

$$R_1 = \frac{V_{OH} - V_{BE}}{I_B}$$

$$= \frac{4.8 - 0.5}{5mA} = \frac{4.3}{10^{-3} \times 5} = 8600 \Omega$$

Standard value = 8200Ω and 390Ω

Alarm (Hourly)

A 7485 comparator was used. This is because it can be able to compare the minute digit in the clock note when $A=B$ and then, give a high in the output. The output is then fed into the reset pin of a 555 timer.

$$F = \frac{1}{T}$$

$$C = \frac{1.44}{(R_A + 2R_B)c}$$

Frequency of 1 KHz was required to be generated by the 555 timer and so the resistor values were

$$R_A = 1K\Omega$$

$$R_B = 100K\Omega$$

$$= \frac{1.44}{1000 + 200000} = 7.16 \mu F$$

Standard capacitor value = $47 \mu F = 44.1 \mu F$

Standard capacitor value = $47 \mu F$

Time Base (Pulse Generator)

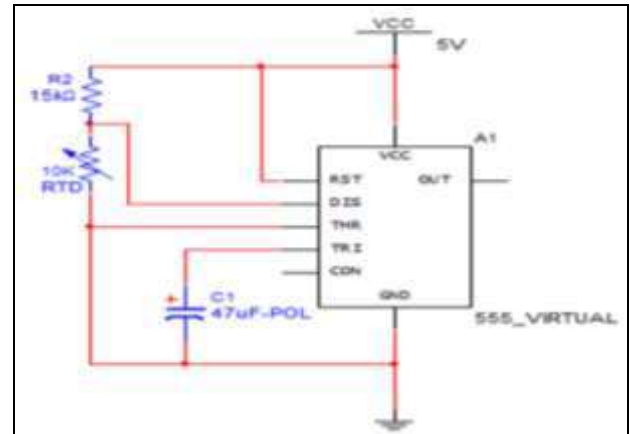


Fig 5: 555 Timer (monostable)

One cycle consist of one charge time and one discharge time. The RC time constant for charge is $C (R_A + R_B)$ because capacitor charge through both R_A and R_B , but discharge through R_B only $R_B C$ because capacitor discharge through R_B only. Therefore, the charge time will be longer than the discharge time because of the different in the RC time constants. With this knowledge in hand I can construct an equation for the total time of one cycle of the clock.

$$T_c = 0.69(R_B + R_A) C$$

$$T_{DC} = 0.69R_B C$$

Where

T_c = Time to charge the middle $\frac{1}{3}$ of V_{cc}

T_{DC} = Time to discharge the middle $\frac{2}{3}$ of V_{cc}

Therefore time for one cycle (P) is

$$T = T_c + T_{DC} = 0.69 (R_A + R_B) C + 0.69R_B C$$

Where T = period

The frequency of a clock (f) = Reciprocal of a period P.

$$F = \frac{1}{T_p} = \frac{1}{0.69(R_B + 2R_A)c}$$

$$R_A = 1.2K\Omega$$

$$R_B = 1.7K\Omega$$

$$C = 10 \mu f$$

$$T_c = 0.69 (1.2 + 1.7) \times 10^3 \times 10 \times 10^{-6}$$

$$= 0.0200$$

$$T_{DC} = 0.69 \times 1.7 \times 10^3 \times 10^{-6} = 0.0117$$

$$F = \frac{+1}{T}$$

$$T = T_c + T_{DC} = 0.0200 + 0.0117$$

$$T = 0.0317$$

$$F = \frac{1}{0.0317} = 31.5Hz$$

Counters

A 7490 IC was used in this journal. The package may be programmed to be a decade counter and can count up to 10. The one pulse per second signal is fed into second section which is used to count second from 0-59 for the minute will count from 0-9. After 9 counts, the BCD counter recycles to 0 which triggers the divide by 6 counter is 0101 (5) counts and the divide by 10 counter is 1001 (9), so that the display reads 59 minutes. Next pulses, recycles the divide by 10 counters and divide by 6 counters (both recycles every 60 minutes).

Table 1: Hour Unit Decade Counter

Divide By 6				Divide By 10			
QD	QC	QB	QA	QD	QC	QB	QA
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1

The above truth tables fully describe how the resetting from 23:59:59 to 00.00.00 is achieved. The 7490 output QB of the divide by 6 counter is connected to one input of the AND gate at the second count of the divide by 6 and fourth count of the divide by 10, the output of the 7490 counters are connected to the output of the AND gate. This implies that one the 24th hour is detected, the output of the AND gate becomes high thereby resetting the counters to 00:00:00.

$$R = \frac{V_{cc} - V_{rated}}{I_{rated}}$$

Where

V_{rated} = Minimum voltage that can turn ON the LED

I_{rated} = Minimum current that can turn ON the LED

$$R_1 = \frac{5 - 2.5}{10^{-3}} = 250 \Omega$$

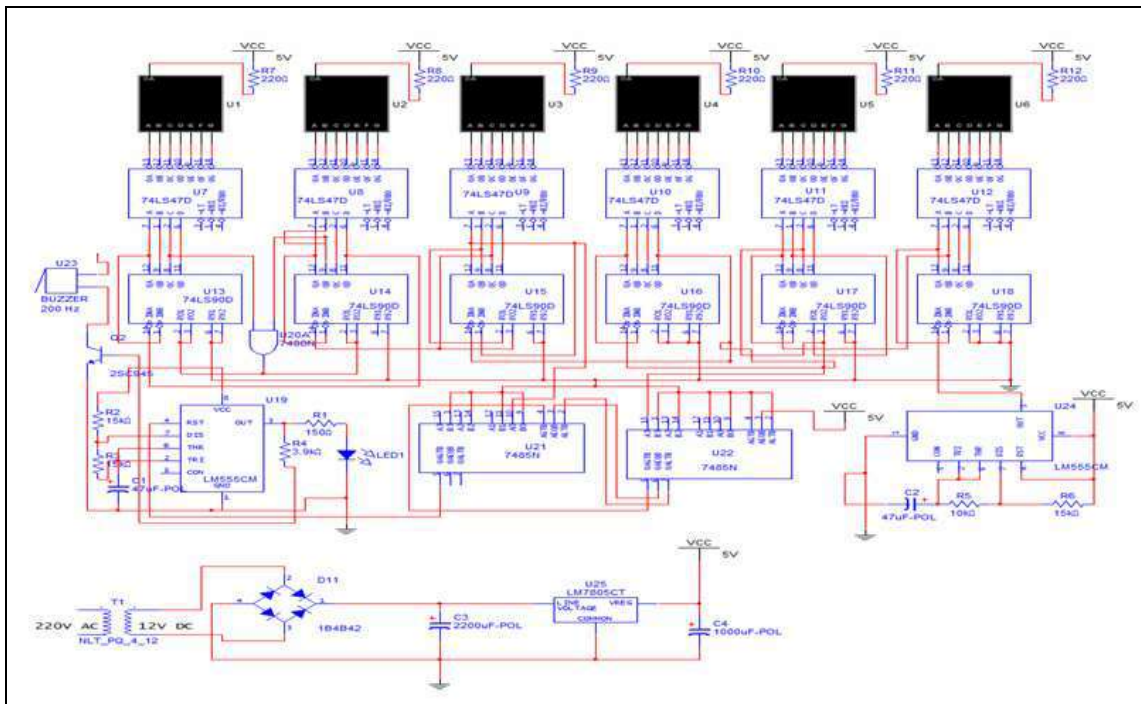


Fig 6: Circuit diagram of digital clock with hourly alarm



Fig 7: Hardware Internal circuitry of digital clock with hourly alarm

Conclusion

The aim of the project, which is to design and construction a digital clock with hourly alarm using common electronic components such as counters, decoders, 7-segment displays, logic circuit, etc. to achieved high level of accuracy in time recording, was successful.

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