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Design and implementation of 6T SRAM cells using cadence virtuoso

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Abstract
This paper presents the design and analysis of a low-power 6-transistor (6T) Static Random Access Memory (SRAM) cell using 180nm CMOS technology in the Cadence Virtuoso environment. The objective is to achieve functional stability, minimal power consumption, and an optimized layout suitable for academic and embedded applications. Reliable read/write operations are ensured by proper transistor sizing and structural optimization. Performance evaluation, via transient and DC simulations, highlights write/read behavior, signal integrity, and power efficiency. The butterfly curve method estimates the Static Noise Margin (SNM). Layout verification is performed using Design Rule Check (DRC), Layout Versus Schematic (LVS), and parasitic extraction. Results confirm the suitability of the 180nm process for low-power SRAM with a balanced trade-off between stability, area, and efficiency. Voltage swing and internal node behavior are examined to ensure logic retention. This study demonstrates the practical relevance of 180nm technology for memory design and academic research.

Keywords: 6T SRAM, 180nm CMOS, DRC, LVS, cadence virtuoso, low-power design, layout design, parasitic extraction

1. Introduction
The growing demand for high-speed and energy-efficient digital systems has intensified the focus on reliable and compact memory architectures. Among these, Static Random Access Memory (SRAM), particularly the 6-transistor (6T) cell, remains a widely adopted solution because of its fast access time, low latency, and stability under powered conditions. SRAM is extensively integrated into microprocessors, cache memories, and embedded systems where performance and power efficiency are critical. While advanced technology nodes below 100nm dominate commercial VLSI development, the 180nm CMOS process continues to hold significant value in academic research and prototyping. Its advantages include process stability, manageable design complexity, and reduced sensitivity to fabrication variations, making it ideal for foundational learning and low-cost implementation. In this work, a 6T SRAM cell is designed and implemented using 180nm CMOS technology within the Cadence Virtuoso environment. The design emphasizes stable read and write functionality while minimizing both static and dynamic power consumption. Comprehensive simulations are performed using transient and DC analyses to evaluate key performance parameters such as write delay, internal node voltages, signal transition characteristics, and Static Noise Margin (SNM). SNM is derived using the butterfly curve method based on the maximum square technique. The physical layout of the SRAM cell is developed with careful attention to symmetry, area efficiency, and design rule compliance. Post-layout validation is conducted using Design Rule Check (DRC), Layout Versus Schematic (LVS), and parasitic extraction through Assura, ensuring design correctness and manufacturability.

This study serves as a practical reference for academic memory design projects, illustrating the complete design flow from schematic development to layout verification. By operating at the 180 nm node, designers can clearly observe critical trade-offs such as power versus stability and area versus performance without the added complexity of deep submicron effects. The methodology presented here provides a strong foundation for memory architecture exploration and prepares students and researchers for future scaling into more advanced CMOS technologies.

In addition to its widespread application, SRAM design presents critical challenges related to power consumption, noise immunity, and process scalability. Designing an efficient 6T cell requires careful trade-offs between transistor sizing, voltage levels, and layout symmetry to ensure robust operation under practical conditions. In low-power systems, minimizing static and dynamic power is essential to improve energy efficiency and reduce thermal impact. Furthermore, SRAM stability under process, voltage, and temperature variations is vital for system reliability. Conducting this work at the 180nm node enables clearer visualization of these trade-offs while offering accessibility for circuit-level experimentation. The insights gained through this work contribute to foundational learning and support the development of more complex memory architectures in future research. Moreover, by including detailed simulation analysis and layout verification, this study offers a comprehensive framework for academic design. The methodology followed can serve as a reference for future SRAM implementations at other technology nodes and encourages hands-on exploration using industry-standard tools.

2. Literature review

Static Random Access Memory (SRAM) continues to play a crucial role in high-performance digital systems, with its efficiency directly impacting processor speed, power consumption, and overall reliability. Among various SRAM architectures, the 6-transistor (6T) configuration remains the most widely implemented due to its simplicity, fast access times, and suitability for integration in cache memory, microcontrollers, and embedded systems. In recent years, extensive research has been conducted to optimize the 6T SRAM design by improving its power efficiency, read/write stability, and layout compactness.

Although the focus of industrial applications has largely shifted toward advanced technology nodes such as 45nm and 28nm, the 180nm CMOS process continues to offer unique advantages in educational and prototyping environments. These include ease of fabrication, cost-effectiveness, and better design observability making it ideal for circuit-level learning and research

Mukesh Kumar and Jagpal Singh Ubhi [1] presented a comparative study on 6T, 7T, and 8T SRAM designs using the 180nm node, where they found that an optimized 6T cell offers favorable trade-offs in terms of area, power, and SNM, making it suitable for applications with moderate performance demands. Similarly, Ranjan and Maskara [2] analyzed SRAM behavior at both 45nm and 180nm nodes. Their findings revealed that although advanced nodes provide better speed and lower dynamic power, the 180nm node exhibits greater stability and reduced sensitivity to process variations, which is beneficial for analog or low-frequency digital systems. In another study, Sharma and Devashrayee [3] implemented a 6T SRAM cell using the Cadence Virtuoso toolchain at 180nm. Their work emphasized successful completion of design verification steps like DRC and LVS, highlighting the practicality of this technology node for academic experimentation. Further research by C. Ashok Kumar *et al*. [4] compared low-power SRAM performance across 180nm and 90nm nodes, concluding that while scaling improves integration density, 180nm offers better noise immunity, simpler modeling, and more reliable pre-silicon verification due to weaker short-channel effects.

Collectively, these studies reaffirm the significance of 180nm technology for instructional design, early-stage VLSI research, and small-scale chip development. However, many of these works focus on individual aspects of SRAM design, such as simulation or layout, rather than providing an end-to-end design flow. The present work addresses this gap by presenting a complete design and analysis framework for a 6T SRAM cell at 180nm. This includes schematic design with precise transistor sizing, transient and DC simulations, SNM evaluation, power estimation, and complete layout verification through DRC, LVS, and parasitic extraction using the Cadence Virtuoso platform.

3. Design Methodology

The 6-transistor (6T) SRAM cell was designed using 180nm CMOS technology within the Cadence Virtuoso platform. The core of the SRAM cell comprises two cross-coupled CMOS inverters that form a bistable latch, along with two access NMOS transistors controlled by the Word Line (WL). These access transistors facilitate the interaction between the internal storage nodes and the Bit Lines (BL and BLB), enabling data transfer during read and write operations. A conceptual view of the cell structure is shown in Figure 1.

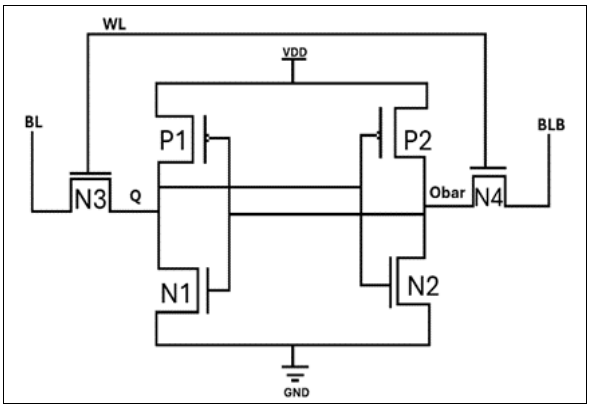

Fig 1: 6T SRAM architecture design for 180 nm technology

In this architecture, the internal nodes Q and $\bar{Q}$ (complement of Q) represent the binary data stored in the cell. The cross-coupled inverters maintain the logic state, while the WL signal controls whether the access transistors connect these nodes to the bit lines. During a write operation, the bit lines force the desired value into the latch. During a read, the internal node state influences the voltage swing on the bit lines, which is sensed externally. Transistor sizing is critical to balancing read stability, write margin, and leakage power. In this design, the pull-down NMOS transistors are sized larger to ensure stronger '0' retention during reads, while the access NMOS transistors are optimized to provide sufficient drive strength without disturbing the stored value. The pull-up PMOS transistors are sized relatively smaller to improve writability. This sizing methodology ensures robust operation across process and voltage variations. Once the schematic was completed, simulations were conducted using both transient and DC analyses. Transient simulations were used to observe dynamic behavior during read and write operations, extracting timing parameters such as signal rise and fall time, read/write delay, and peak-to-peak voltage variations at the output node (Q). DC analysis focused on Static Noise Margin (SNM), obtained via butterfly curves,

and validated the bistable operation of the cell under nominal conditions. After functional validation, the layout was created in the Cadence Layout Editor with careful attention to symmetry, minimal area, and proper diffusion sharing to reduce parasitics. Post-layout verification included Design Rule Check (DRC) to ensure geometrical correctness, Layout Versus Schematic (LVS) to confirm netlist integrity, and Assura-based parasitic extraction (AV) to capture real-world performance impacts. This comprehensive design flow ensures that the SRAM cell is not only functionally correct but also optimized for low-power operation and manufacturability at the 180 nm technology node.

4. 6T SRAM AT 180NM

At the 180nm technology node, precise transistor sizing plays a key role in achieving stable memory operation, fast switching response, and reduced power consumption. The designed 6T SRAM cell consists of two cross-coupled CMOS inverters forming a bistable latch and two NMOS access transistors responsible for data transfer to and from the bit lines. The pull-down NMOS transistors (N1, N2) are sized with a width of 3 µm and a length of 180 nm, providing strong drive capability for holding logic '0' during read operations. The access transistors (N3, N4), which connect the internal storage nodes to the bit lines (BL and BLB), are given dimensions of 2 µm / 180 nm to balance write access and cell stability effectively. The pull-up PMOS transistors (P1, P2) are designed with a width of 1.5 µm and the same channel length, providing adequate pull-up strength while minimizing static power dissipation. These sizing ratios are selected to ensure robust operation under nominal supply voltage conditions, enabling successful read and write operations without data disturbance. The complete schematic of the 6T SRAM cell is illustrated in Figure 2.

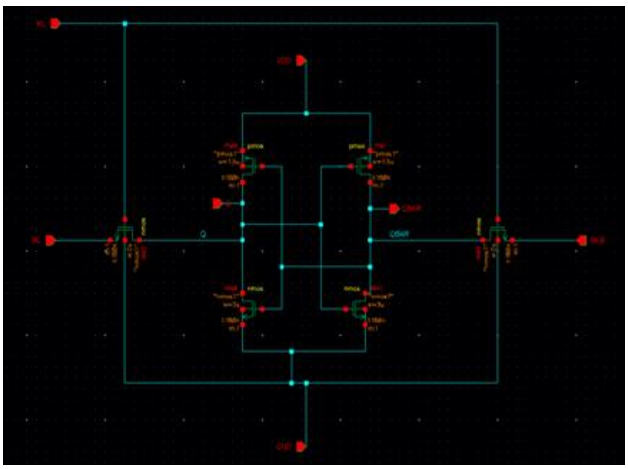

Fig 2: Schematic design of 6T SRAM at 180 nm technology

4.1 Transient Analysis

Transient simulations were carried out to analyze the dynamic switching behavior of the SRAM cell during write and read operations. The cell demonstrated correct and stable performance while storing and updating logic states, thereby confirming its functionality under typical switching conditions. During the active write cycle, the measured dynamic power consumption was approximately 1.338 µW indicating energy-efficient operation. The waveform corresponding to the write cycle is illustrated in Figure 3.

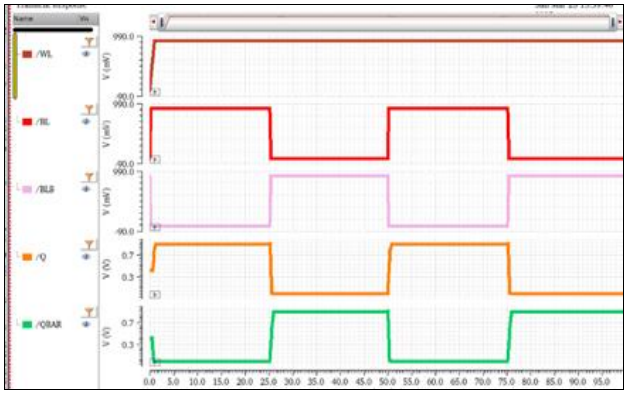

Fig 3: Transient response of write operation

For the read cycle, shown in Figure 4, the Word Line (WL) is asserted to activate the access transistors, while both bit lines (BL and BLB) are precharged to the supply voltage of 900 mV (VDD). If the cell stores a logic '1', the internal node Q remains high and $\bar{Q}$ stays low, allowing data to be sensed without disturbing the stored value. This confirms a non-destructive read operation, with proper transistor sizing contributing to improved read margin and overall reliability.

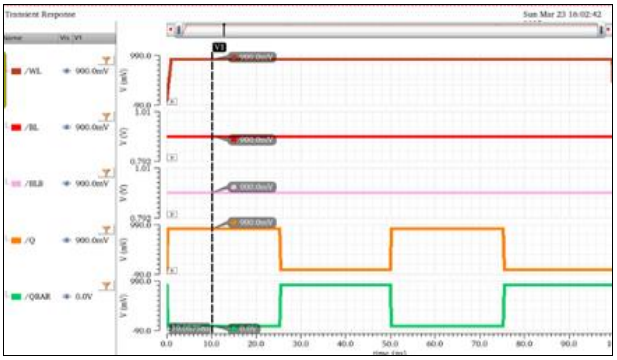

Fig 4: Transient response of read operation

4.2. DC Response

The DC simulation was performed to assess the steady-state behavior and noise resilience of the SRAM cell at a supply voltage of 0.9 V. The Static Noise Margin (SNM), a critical metric for ensuring data stability, was extracted using the butterfly curve method and measured at approximately 200 mV. This value reflects the cell's robustness against external noise and confirms the proper bistable operation of the internal storage nodes. During the DC sweep, node Q settled at 414 mV, while node $\bar{Q}$ reached 407 mV, verifying symmetrical operation. The SNM was determined using the maximum square method, as shown in the butterfly plot in Figure 5.

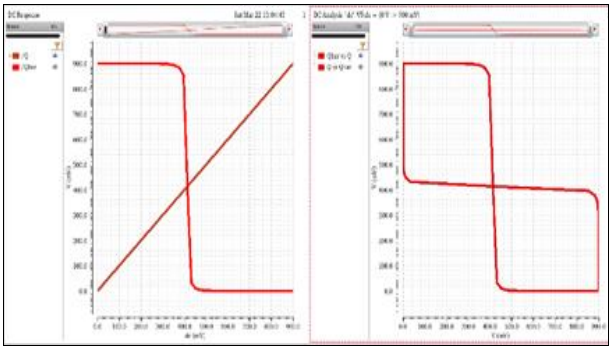

Fig 5: SNM butterfly curve extracted from DC response

Static power consumption arises from leakage currents when the SRAM cell is in standby mode, with no active switching occurring. In this design, the static power was measured to be approximately 21.81 µW, which aligns well with expected leakage behavior at the 180nm CMOS technology node. This value reflects the inherent leakage through the transistors when they are biased in a steady state but not toggling. Figure 6.1 illustrates the static power profile obtained from the DC simulation setup

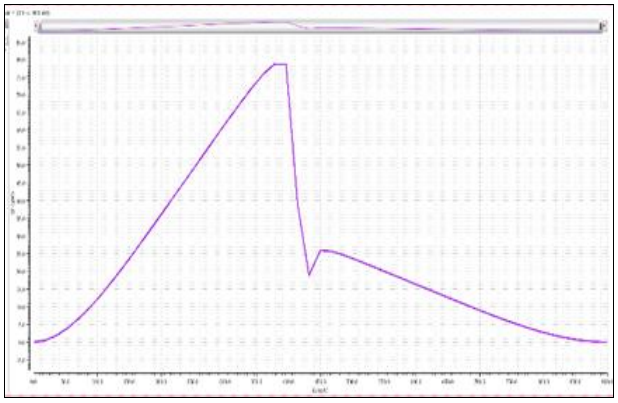

Fig 6.1: Static power consumption curve

Dynamic power consumption occurs during switching activity in the SRAM cell, particularly during read and write operations. It is primarily due to the charging and discharging of internal node capacitances as transistors switch states. In this design, the dynamic power was calculated to be approximately 1.338 µW based on the transient simulation results. This value is consistent with expected dynamic behavior in 180nm CMOS technology under moderate switching activity and a 0.9 V supply voltage. The result confirms that the circuit demonstrates efficient switching characteristics with low dynamic power dissipation. Figure 6.2 illustrates the dynamic power profile as observed from the transient simulation.

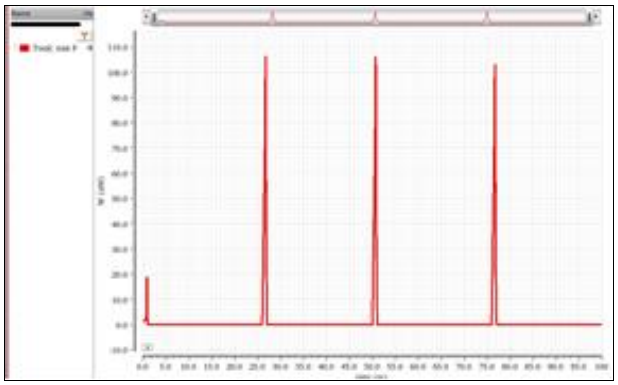

Fig 6.2: Dynamic power consumption curve

4.3 Layout Design and Optimization

The physical layout of the 6T SRAM cell was implemented using Cadence Virtuoso, adhering strictly to the 180nm CMOS design rules. The final layout occupied an area of approximately 234.228 µm² and was constructed with careful consideration for layer alignment, proper spacing, and manufacturing constraints. Transistor placement and routing were optimized for symmetry, area efficiency, and functional accuracy, reducing the risk of layout-induced mismatches or parasitic issues. The completed layout is shown in Figure 7. To validate the physical design, a series of post-layout verification steps were performed. Design Rule Check (DRC) confirmed adherence to process-specific geometric constraints, while Layout Versus Schematic (LVS) verified that the layout's netlist matched the intended schematic connectivity. Additionally, Assura-based parasitic extraction (AV) was conducted to estimate the layout-induced resistance and capacitance, enabling a more realistic evaluation of post-layout performance.

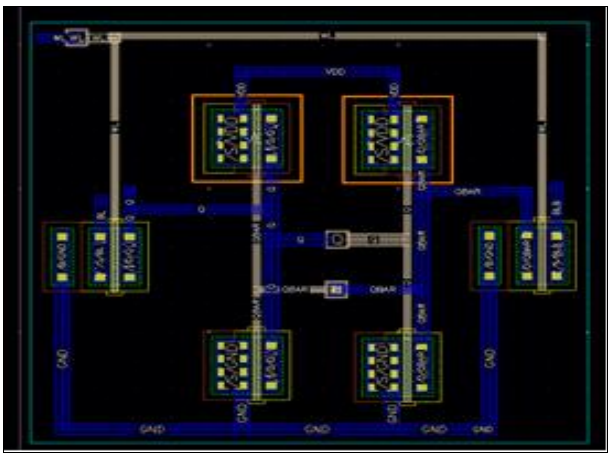

Fig 7: Layout Design

4.4 Design Rule Check

The finalized layout of the 6T SRAM cell was verified through Design Rule Check (DRC) using the Cadence Assura tool. This step ensures compliance with all geometric and manufacturing constraints defined by the 180nm CMOS design rules, including minimum spacing, layer widths, enclosures, and overlaps. Performing DRC is essential to guarantee that the layout can be fabricated reliably without encountering violations that could lead to yield loss or circuit malfunction. A DRC-clean status indicates that the design adheres to all physical requirements set by the foundry. The validated layout, free from rule violations, is shown in Figure 8.

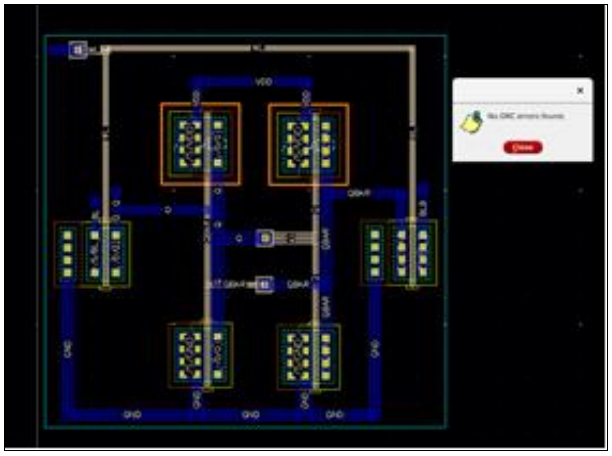

Fig 8: DRC verification of 6T SRAM layout at 180 nm

4.5 Layout Versus Schematic (LVS)

Following the successful DRC, a Layout Versus Schematic (LVS) check was conducted using Cadence Assura to verify the logical equivalence between the physical layout and the schematic design. This step ensures that all devices, nodes, and interconnections in the layout precisely match those

defined in the schematic netlist.

A clean LVS result confirms that the layout correctly implements the intended circuit functionality and is free from errors such as missing or extra components, incorrect pin connections, or mismatched device properties. Achieving LVS match is a critical milestone before proceeding to fabrication. The LVS confirmation for the 6T SRAM layout is depicted in Figure 9.

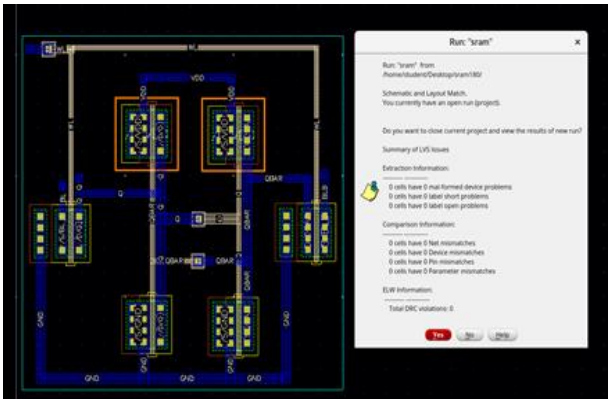

Fig 9: LVS Verification Result for 6T SRAM Layout

4.6 Assura-Based Parasitic Extraction

The final stage of layout verification involved performing parasitic extraction using the Assura (AV) tool. This process calculates the parasitic resistances and capacitances introduced by metal interconnects, diffusion regions, and routing layers within the physical layout. These extracted parasitics are crucial for accurate post-layout simulations, as they can significantly influence timing, signal integrity, and power consumption.

By incorporating these layout-induced effects into the net list, designers can evaluate the circuit's real-world behavior more precisely. The extracted view showing parasitic elements overlaid on the layout is illustrated in Fig. 10. This step ensures that the impact of layout-level imperfections is accurately reflected in the simulation results. It also helps identify any performance degradation or signal delay caused by parasitic loading, enabling more informed design optimization.

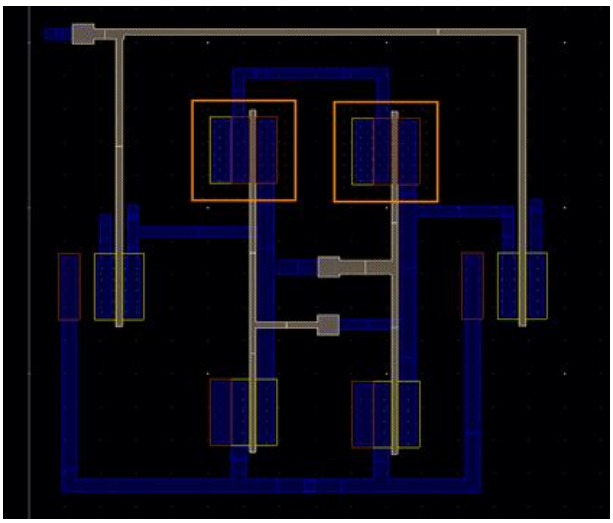

Fig 10: AV Extraction View

5. Simulated Results

The performance of the designed 6T SRAM cell using the 180nm CMOS technology was thoroughly evaluated through DC and transient simulations in the Cadence Virtuoso environment. Key performance metrics were extracted to analyze the cell's stability, switching behavior, and power efficiency. Critical parameters such as the Static Noise Margin (SNM), internal node voltages, read/write delay, static leakage, dynamic power dissipation, and the total layout area were examined. These results demonstrate the functional correctness and energy efficiency of the design, validating its suitability for low-power memory applications, particularly in academic, educational, and prototype-level platforms. The evaluation highlights the practical viability of the 180nm node for foundational SRAM design and research-oriented VLSI development.

Table 1: Performance summary for 6T

Parameter	180 nm
Supply Voltage (mV)	900
peak-to-peak voltage	905.5 mV
SNM (V)	200mV
Node Voltage Q (mV)	420
Node Voltage $\overline{Q}$ (mV)	422
Static Power (µW)	21.81
Dynamic Power (µW)	1.338
Layout Area (µm²)	234.228

SRAM Cell

Static vs dynamic power dissipation

To better understand the power behavior of the designed SRAM cell, both static and dynamic power values were plotted side by side. As shown in Figure 11, the static power consumption was significantly higher at 21.81 µW, compared to the dynamic power consumption of 1.338 µW. This is expected since static power accounts for continuous leakage even during standby, whereas dynamic power arises only during switching events. The results highlight that leakage dominates the total power budget in standby mode, especially at lower supply voltages such as 0.9 V in 180nm technology.

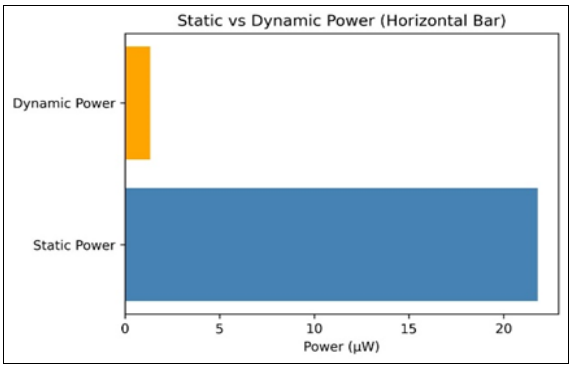

Fig 11: Comparison of static and dynamic power consumption

Peak-to-peak voltage vs node voltage

To evaluate the dynamic behavior of the SRAM cell compared to its steady-state condition, the peak-to-peak voltage swing during transient operation was compared with the DC voltages at internal nodes Q and $\overline{Q}$. As illustrated in Figure 12, the output node Q exhibited a peak-to-peak voltage of approximately 905.5 mV, nearly equal to the supply voltage of 0.9 V, indicating strong switching capability and full voltage swing. In contrast, the DC operating points of nodes Q and $\overline{Q}$ were found to be 420 mV

and 422 mV, respectively. This reflects the balanced nature of the cross-coupled inverters during the hold state and confirms the cell's ability to retain logic values with minimal voltage offset.

The small difference between the Q and $\bar{Q}$ node voltages in DC confirms the proper stability of the SRAM cell in standby mode. The large peak-to-peak swing observed during transient operation demonstrates the circuit's ability to perform fast and reliable read/write transitions. Such characteristics are essential for ensuring high noise margins and strong logical levels in memory applications.

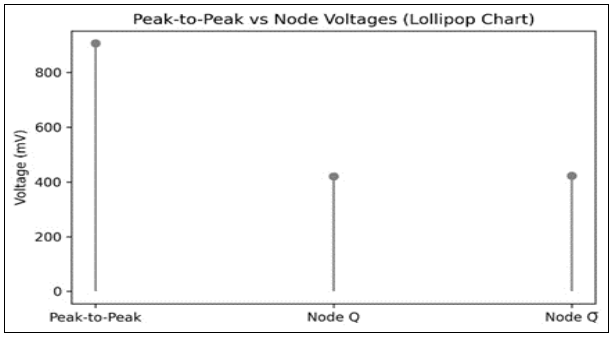

Fig 12: Comparison of peak-to-peak voltage and node voltages at Q and $\bar{Q}$

Conclusion

This work presents the complete design, simulation, and layout verification of a low power 6T SRAM cell using 180nm CMOS technology in the Cadence Virtuoso environment. The proposed architecture demonstrates reliable read and write operations achieved through careful transistor sizing and layout optimization. Comprehensive transient and DC analyses confirm strong signal integrity, robust data retention, and efficient power performance. The measured static and dynamic power dissipation values, along with satisfactory Static Noise Margin (SNM), validate the suitability of the chosen process node for academic and prototype memory designs. Layout-level checks, including DRC, LVS, and parasitic extraction, further ensure manufacturability and real-world feasibility. Overall, this study illustrates the practical relevance of the 180nm node for instructional VLSI projects and serves as a reference framework for future SRAM research and development using industry-standard tools.

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